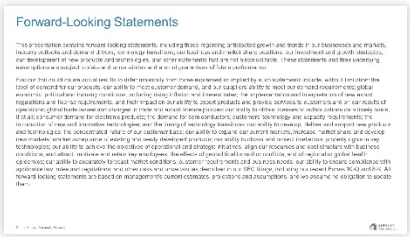
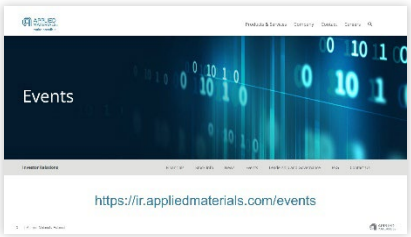
2023 WFE Market Summary

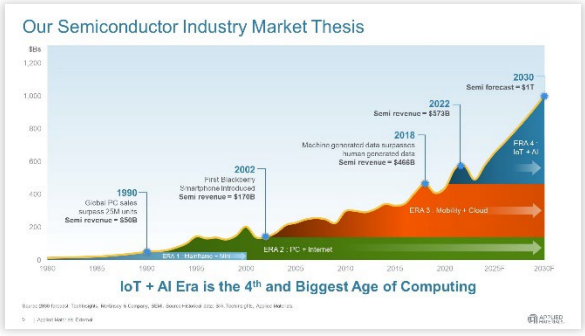
KEY POINTS | MAY 2, 2024





Agenda:

- One, our perspective on the growth of the semiconductor industry we serve, and the evolution of the wafer fab equipment market we participate in.
- Two, official third-party sizing of the fab equipment market in 2023, which became available just recently. Our proprietary analysis of the market by semiconductor device type.
- Three, Applied's technology portfolio, where we compete in the overall market, how we deliver our technologies to customers, and how we're performing in those areas. Our share by semiconductor device type and our analysis of high-bandwidth memory manufacturing.
- Four, our strategy and how we see the AI and IoT market inflections changing the landscape of the equipment industry in the years ahead, particularly as logic density improvement shifts from lithographic scaling to lithography plus materials-enabled scaling, including in gate-all-around transistors, backside power and advanced packaging.



- A number of frameworks have guided our thinking about the semiconductor and equipment markets since around 2017.

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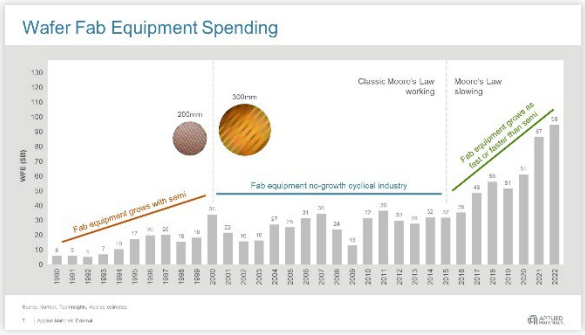
- We first showed this slide at our 2021 investor meeting more than three years ago.
- This framework suggests that we are in the fourth major era of computing which we call AI and IoT.
- Each era more than doubles the size of the semiconductor industry, and the current era will drive the market to a trillion dollars according to multiple third-party forecasts.

- Here is a more precise look at semiconductor industry revenue from 1990 through 2023 per TechInsights and Gartner.
- Over this period, the industry experienced relatively steady, cyclical growth driven by PCs and the Internet; then mobility and cloud computing; and most recently AI and IoT.



- We contrast the previous pattern with the growth of the equipment industry over the same period and note three distinct phases.
- From 1990 through 2000, the equipment industry more-or-less tracked the semiconductor industry.
- From 2000 -- which is when 300mm wafers came into the industry -- through around 2015, equipment became a no-growth, cyclical industry.
- The industry broke out of this pattern around 2015, growing with the semiconductor industry, and at times growing faster than the semiconductor industry.
- Next is what we think drove this inflection.

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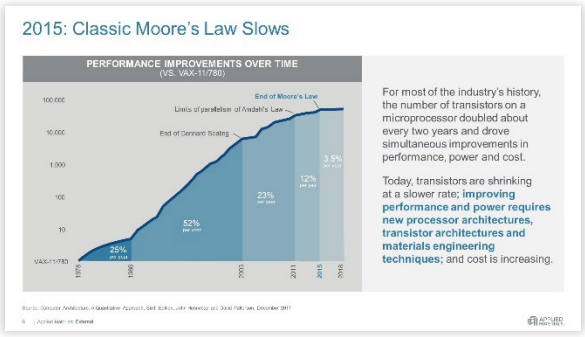
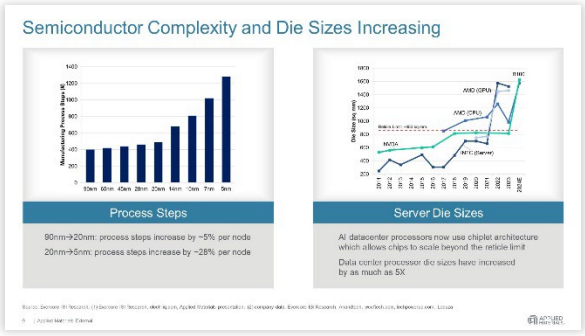


- The sixth edition of a computer architecture textbook by Professors Patterson and Hennessey included this illustration which declared the end of Moore's Law in 2015.
- 2015 is around the time it became harder for classic Moore's Law to deliver twice the number of transistors in a given-sized die about every two years, and particularly to do so with improvements in performance and power.



- The industry has needed to adapt to the slowing of classic Moore's Law scaling.
- The number of steps needed to make a leading-edge chip began to increase, as seen on the chart on the left.
- Specifically, more steps are needed to build 3D FinFET transistors as well as to create new kinds of wiring that solve electrical resistance issues to enable chip features to shrink and chips to still deliver improvements in performance and power.
- With transistor counts growing at a slower pace, the industry has needed to build bigger chips.
- We can no longer fit all the transistors we need for advanced server chips within the reticle limit, which is the 850-square-millimeter die size limit of lithography systems.
- It can now require more than one chip to make a high-end server processor.

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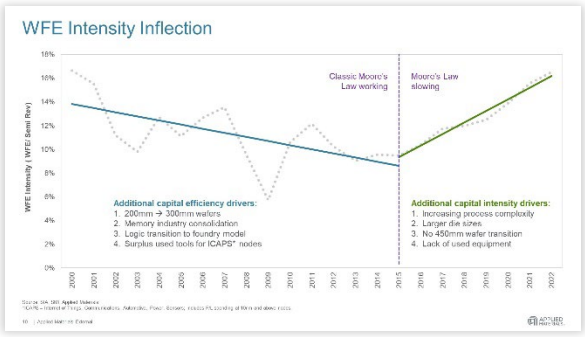

- This chart examines equipment capital intensity from 2000 through 2022.
- Equipment capital intensity was around 17% in 2000 and declined to about 9% at around the time classic Moore's Law slowed. It has recovered since then.
- The opposing trendlines can be explained: equipment capital intensity declined from 2000 for at least five reasons.
  1. Classic Moore's Law worked nicely.
  2. 300mm wafers gave chipmakers a 125% increase in the number of like-sized chips on every wafer produced.
  3. The memory industry consolidated, making it more capital efficient.
  4. Given the high cost of 300mm fabs, many logic makers transitioned to the foundry model, making the logic market more capital efficient as well.
  5. When memory and logic chipmakers exited manufacturing, their equipment was sold into the used equipment market and allowed ICAPS[1] chipmakers to buy equipment at a fraction of the price of new equipment.
- From 2015 onwards, capital intensity increased for a variety of reasons, notably these.
  1. Moore's Law slowed.
  2. Process complexity increased.
  3. Die sizes increased.
  4. Throughout the longer history of the industry, when capital intensity increased, a new wafer size was introduced, resetting it lower. The industry began a transition to 450mm wafers, but it was not implemented.
  5. The growing ICAPS market absorbed the excess used equipment. This factor is important because the ICAPS market drives 50% or more of total semiconductor industry revenue, and when ICAPS chipmakers buy new equipment instead of used, their equipment capital intensity increases.
- We believe that in the future, the equipment industry can continue to grow as fast or faster than the semiconductor industry on a [1]through-cycle basis.
- We believe equipment capital intensity is likely to remain at higher levels in the future than in the past period (through 2015) shown on this chart, also on a through-cycle basis.

[1] ICAPS = Internet of things, communications, automotive, power and sensors.

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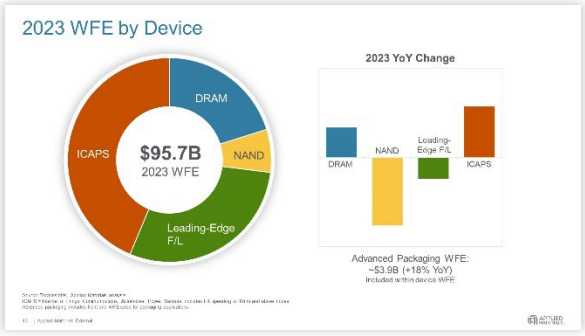
- Recently, TechInsights published this report.
- WFE spending was $95.7B in 2023, up 1% from 2022.
- 2023 WFE was also 3 times higher than 2015 WFE, which is around the time classic Moore's Law slowed.
- Applied was #2 in WFE revenue in 2023.



- This is our analysis of fab equipment spending by semiconductor device type.
- The information is from our internal analysis, which is based on our broad view of the marketplace.
- Foundry-logic grew in 2023, with ICAPS higher year-over-year and leading-edge foundry-logic lower.
- In memory, DRAM grew while NAND declined and had the lowest year in nearly a decade.
- In aggregate, memory was around 25% of WFE, lower than the one-third ratio that we believe is appropriate for the foreseeable future.
- Packaging drives front-end equipment spending across all the device segments, and we believe it drove $3.9 billion dollars in spending for the year.

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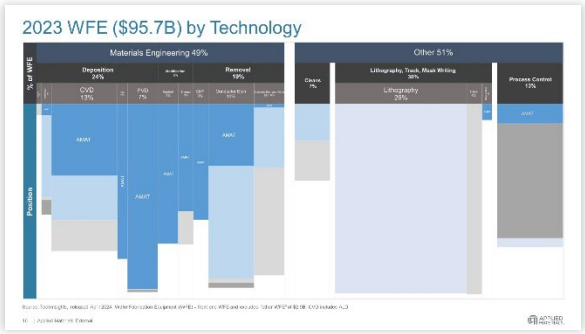
- Broadly speaking, Applied Materials focuses on materials engineering, which is creating and depositing materials; shaping and removing materials; and modifying materials -- as well as connecting chips with advanced packaging.
- In addition, Applied participates in several key areas of the process control segment.
- There is strong synergy between materials engineering and eBeam metrology where we have the #1 position in the industry.
- Our eBeam technology lets us see and measure the outcomes of our materials engineering steps with nanometer precision, which helps us continuously improve.



- This is the $95.7-billion-dollar WFE market segmented by technology.
- Materials engineering composed 49% of WFE in 2023.
- Cleans represented 7% of WFE in 2023, and Applied does not participate.
- Litho, track and mask writing was 26% of WFE in 2023, and Applied participated with a modest position in the mask-writing market.

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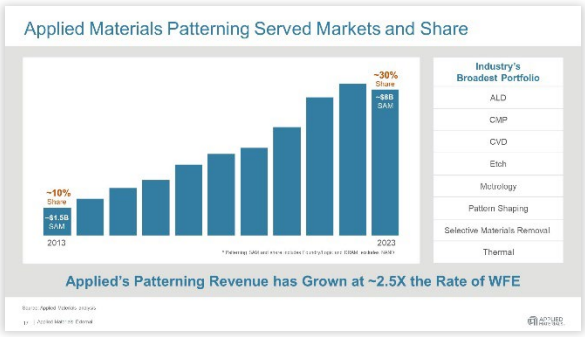
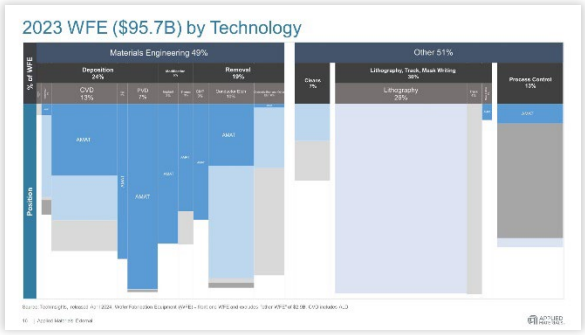
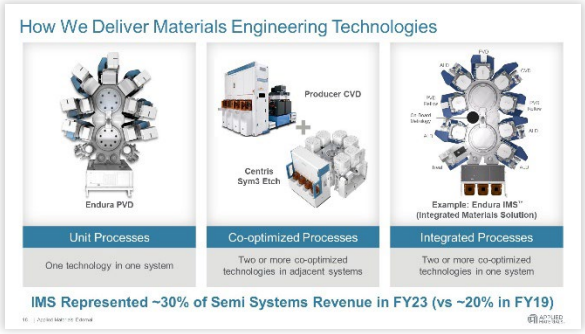


- Lithography helps create patterns in photoresist.
- Materials engineering is needed to transfer the patterns into the wafer to make structures like transistors and wiring.
- The materials engineering patterning market plus metrology drove around $8 billion dollars in foundry-logic and DRAM spending in 2023, and Applied's patterning SAM share has grown by 20 points over the past decade to around 30%.

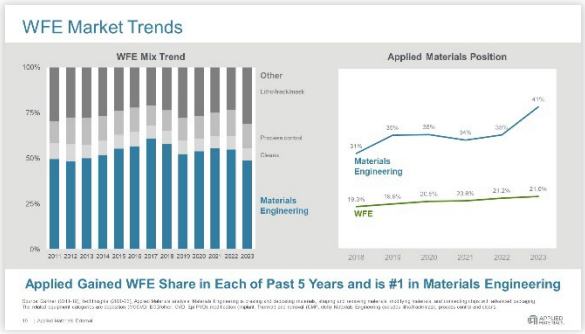


- The process control market drove 13% of WFE in 2023.
- Applied's overall process control share includes our #1 position in eBeam inspection and metrology.
- In summary, materials engineering represents around one half of the WFE market.
- Applied has the #1 share position in materials engineering and the broadest portfolio.



- We deliver materials engineering solutions to customers in three ways.

- One, we sell unit process technology where all of the chambers in the system perform the same process on the wafer. This is the conventional approach which leaves customers with the highest burden of responsibility for process integration.
- Two, we sell cooptimized process technology where two or more adjacent steps are engineered to precision but performed in separate systems. These solutions can give customers better outcomes and faster time to market.
- Three, we sell integrated process technology where 2 or as many as 6 or 7 adjacent steps are engineered to precision and performed in the same system, under pristine, high-vacuum conditions.
- These integrated solutions are critical to delicate transistors and wiring where the materials are so thin and pure that exposure to the atmosphere can negatively impact chip performance, power and yield.
- In fiscal 2019, they drove around 20% of our Semiconductor Systems revenue; in 2023, they drove around 30%.
- Cooptimized solutions and integrated solutions exist across many areas of chipmaking, from EUV and DRAM patterning to transistor formation, transistor contacts, chip wiring and advanced packaging.
- We also have a growing portfolio of integrated materials solutions for the ICAPS market.
- In summary, our cooptimized and integrated solutions help us form close relationships with the world's leading chipmakers, from R&D to sales to high-volume manufacturing and services.



- Our technology and strategy lead to market share gains and outperformance.
- Materials engineering has consistently been around one half of the WFE market.
- There have been periods when materials engineering gained mix share from the other categories like lithography, notably when NAND technology shifted from 2D shrinking to 3D stacking with materials engineering in the 2013 though 2017 timeframe.
- Lithography captured share from materials engineering when EUV came into the roadmap in 2018 and replaced a number of multi-patterning materials engineering steps with a single litho pass.
- In the future, roadmap inflections may influence the balance between materials engineering and other.
- We expect both categories to remain large and important for the foreseeable future.

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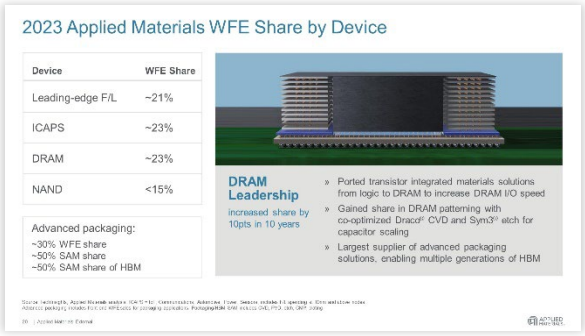
- Applied's share of WFE has increased in each of the past five years to one of the best share outcomes of the past 20 years.
- One of the reasons is patterning, where we have complemented the insertion of EUV in foundry-logic and DRAM with cooptimized CVD patterning films and etch systems.
- Another is wiring where we have used integrated materials solutions to create low-resistance wiring that allows customers to scale to 3nm and beyond with EUV and still achieve high performance and low power.
- Also on the right is our share of materials engineering which exceeded 40% in 2023, in part due to a favorable end market mix.



- This is our 2023 WFE share by semiconductor device type.
- Our share was relatively balanced across leading-edge foundry-logic, ICAPS and DRAM.
- Our WFE share in these markets was in the lower-20-percent range, and we were #1 in materials engineering in all three device segments.
- In 2013, our DRAM share was only around 13%.
- We put a great deal of R&D into cooptimized solutions for DRAM patterning and integrated solutions for DRAM transistors and wiring, and our share grew 10 points higher.
- In NAND, our share was lower than elsewhere mainly because the devices make high use of dielectric etch where we do not compete today.
- We look forward to 3D DRAM which will use conductive materials that play to our materials engineering strengths.
- Advanced packaging has a role in every device type.
- We formed a dedicated group to explore technologies like through-silicon vias around a decade ago and increased our investments several years ago as we anticipated major inflections.
- In 2023 our WFE share of advanced packaging was around 30% and our SAM share was around 50%. We believe our share in high-bandwidth memory was similarly high.

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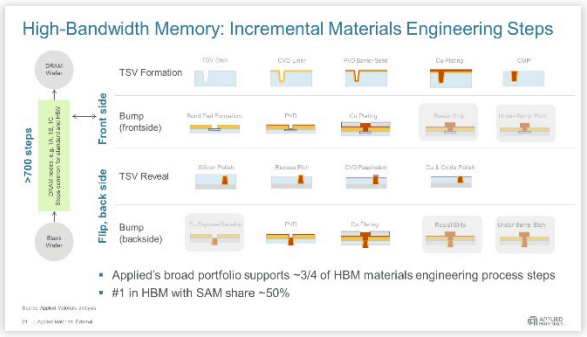

- High-bandwidth memory has an impact on chipmaking and equipment spending.
- On the left, making a DRAM wafer requires about 700 process steps, which are essentially the same for standard DRAMs and HBM.
- DRAM WFE is estimated to be around $9 billion dollars for 100-thousand wafer starts per month of greenfield capacity.
- Around another 5% of WFE spending is needed to create equivalent greenfield capacity to stack the chips using HBM packaging technology.
- On the right, around 10 major materials engineering steps are needed to create through-silicon vias and then contacts on the front side of the wafer, followed by another 9 steps needed to expose the vias on the back side of the wafer and add backside contacts.
- Applied serves around three-quarters of these steps.

- The last section of today's presentation includes frameworks we use to model the future.

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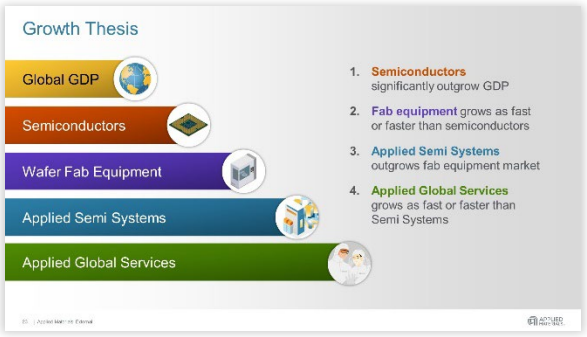
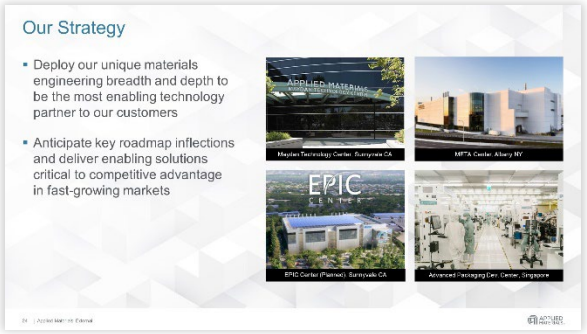


- On our recent earnings calls, we've shared our growth thesis which has four pillars.
- One, we believe semiconductors can outgrow GDP.
- Two, we believe fab equipment can grow as fast or faster than semiconductors on a through-cycle basis due to increasing complexity in the era of AI and IoT.
- Three, we believe Applied's equipment business can continue to outperform the market as major roadmap inflections demand more of our materials engineering technologies.
- We will elaborate on this point in the remainder of the presentation.
- Four, we believe our services business can grow as fast or faster than our equipment business as its revenue compounds with the growth of our installed based which is the largest in the industry.



- This is our strategy for outperforming the market.
- One, we will continue to deploy our unique materials engineering breadth and depth to be the most enabling technology partner to our customers.
- Two, we will continue to anticipate key roadmap inflections and deliver enabling solutions that we believe are critical to our customers achieving competitive advantage in fast-growing markets.
- These are several of our major R&D centers, present and planned, where we collaborate with our customers to enable these inflections.

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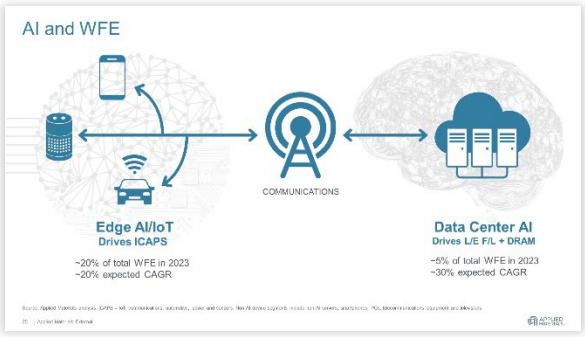
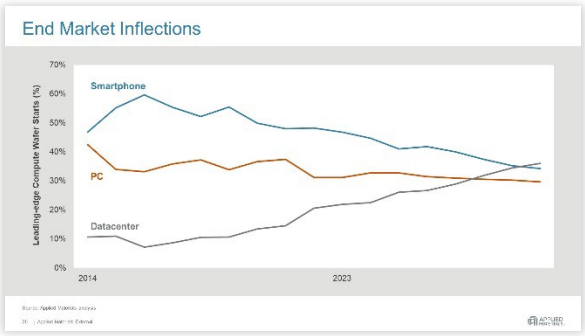


- This is a framework for the wafer fab equipment market in the era of AI and IoT.
- We see AI and IoT as two sides of the same coin.
- The left side creates and transmits data that can be understood and monetized, today primarily on the right side.
- This is the biggest computing era yet, and it is projected by third parties to drive the semiconductor industry to $1 trillion dollars in annualized revenue by the end of the decade.
- We believe this ecosystem drove around 25% of WFE in 2023.
- The right side drove around 5% of WFE.
- The growth rates of AI and IoT era spending are expected to be higher than the overall WFE market, perhaps around 20% on the left side and around 30% on the right which is where we see so much attention today on accelerating generative AI and large language models.



- The trends discussed in this presentation may drive inflections in semiconductor sales and WFE.
- Mobility in the form of smartphones and tablets has been the #1 end market driver of leading-edge foundry-logic and DRAM wafer starts since 2010, with PCs #2 and data center #3.
- Given the expected growth in AI and the semiconductor inflections presented, data center may cross over PCs within the next several years.
- A few years later, data center could surpass mobility to become the #1 driver of leading-edge foundry-logic and DRAM wafer starts.

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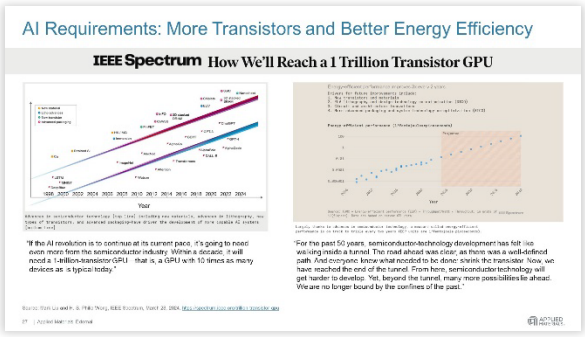
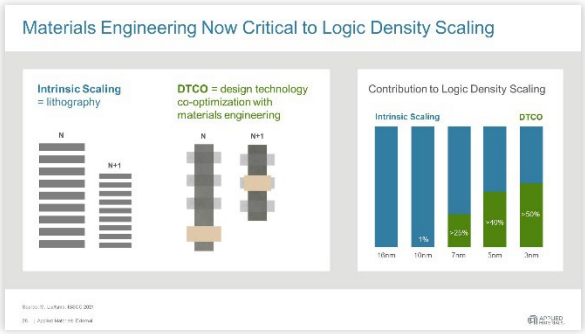
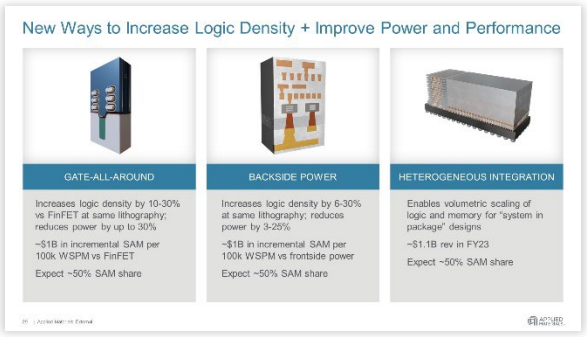


- This article was published around one month ago and authored by Dr. Mark Liu and Dr. H.-S. Philip Wong of TSMC.
- The chart on the left suggests powering the growth of AI models will require new materials, driving EUV lithography even further, new transistors like gate all around, and advanced packaging.
- The chart on the right suggests a need to triple energy-efficient computing every two years, using new transistors and materials, EUV lithography plus design technology co-optimization or DTCO, and more advanced packaging or STCO.
- Applied has already been investing to help drive all of these inflections.



- This chart is based on Dr. Mark Liu's paper at the ISSCC conference in 2021.
- Dr. Liu showed two ways to increase logic density, or the number of transistors on a chip.
- One is intrinsic scaling or shrinking the features using lithography.
- The other is DTCO or design technology co-optimization which is using materials engineering to rearrange the logic features to make them more compact at the same lithography.
- On the right, Dr. Liu showed that at the 3nm node, DTCO with materials engineering is already contributing 50% of the logic density improvements.



- We believe DTCO with materials engineering can go even further.
- We believe the gate-all-around transistor can increase logic density by 10-30% versus FinFET at the same lithography and reduce power consumption by up to 30%.
- We believe backside power can increase logic density by 6-30% at the same lithography and reduce power consumption by up to 25%.
- Heterogeneous integration with advanced packaging is STCO or system technology co-optimization.
- The technique enables the industry to pack what used to occupy much of a circuit board into an integrated 3D chip.
- We call this volumetric scaling whereby we can pack orders of magnitude more transistors into a given space, and shrink the wiring lengths by orders of magnitude, to reduce the electrical resistance and power consumption by orders of magnitude as well.
- Applied has been investing for years to enable these inflections with the broadest materials engineering portfolio, deployed in unit process, cooptimized and integrated solutions.
- The gate-all-around inflection increases our served market opportunity by more than one billion dollars per 100,000 wafer starts per month of greenfield capacity, and we expect SAM share of around 50%.
- The backside power inflection also increases our served market opportunity by more than a billion dollars per 100,000 wafer starts per month of greenfield capacity, and we expect SAM share of around 50%.
- Importantly, we believe integrated materials solutions are the most feasible way to achieve the best logic density scaling of up to 30% at the same lithography.
- This most advanced use of materials engineering can generate the equivalent of around two nodes of lithographic scaling at the same pitch.
- We expect our advanced packaging SAM will grow nicely in the years ahead.
- We expect to maintain the #1 share position in advanced packaging and SAM share of around 50%, both overall and in HBM.

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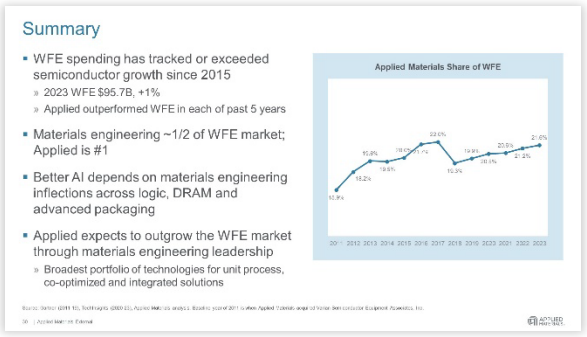

Summary:

- First, we have seen an inflection in the semiconductor equipment industry which transitioned from essentially being a no-growth cyclical industry from 2000 through 2015 to one that has more-or-less tracked or exceeded the growth of the semiconductor industry since around 2015. The WFE market was $95.7 billion dollars in 2023. Applied's unique assets and strategy have enabled the company to outperform WFE in each of the past 5 years.
- Second, one can segment the WFE market into materials engineering and other technologies. Materials engineering has driven around half of spending over many years, and technology inflections can influence the spending mix between materials engineering and other categories.
- Third, materials engineering will play an important role in AI, helping increase both raw performance and energy-efficient performance. AI drives large increases in demand for leading-edge foundry-logic chips, DRAMs and high-bandwidth memory, and Applied has the #1 materials engineering share in all of these devices.
- Fourth, Applied's goal is to continue to outperform the wafer fab equipment industry in the years ahead with our unique assets and strategy.

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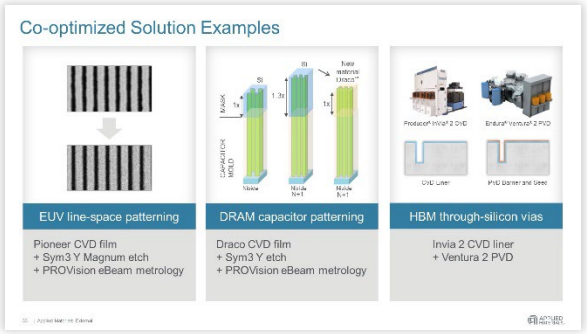
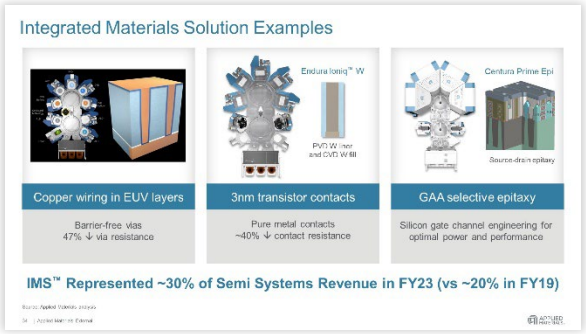
Additional Material:





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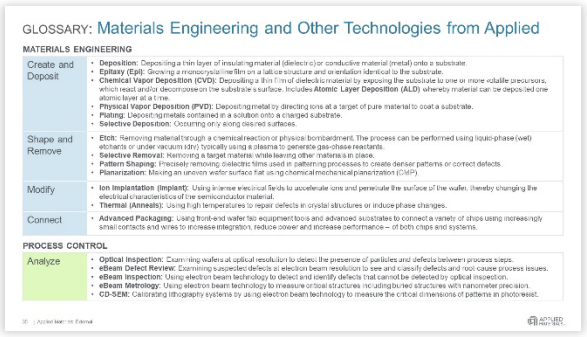

GLOSSARY: Materials Engineering and Other Technologies from Applied

MATERIALS ENGINEERING

Create and Deposit	• **Deposition:** Depositing a thin layer of insulating material (dielectric) or conductive material (metal) onto a substrate. • **Epitaxy (Epi):** Growing a monocrystalline film on a lattice structure and orientation identical to the substrate. • **Chemical Vapor Deposition (CVD):** Depositing a thin film of dielectric material by exposing the substrate to one or more volatile precursors, which react and/or decompose on the substrate's surface. Includes **Atomic Layer Deposition (ALD)** whereby material can be deposited one atomic layer at a time. • **Physical Vapor Deposition (PVD):** Depositing metal by directing ions at a target of pure material to coat a substrate. • **Plating:** Depositing metals contained in a solution onto a charged substrate. • **Selective Deposition:** Occurring only along desired surfaces.
Shape and Remove	• **Etch:** Removing material through a chemical reaction or physical bombardment. The process can be performed using liquid-phase (wet) etchants or under vacuum (dry) typically using a plasma to generate gas-phase reactants. • **Selective Removal:** Removing a target material while leaving other materials in place. • **Pattern Shaping:** Precisely removing dielectric films used in patterning processes to create denser patterns or correct defects. • **Planarization:** Making an uneven wafer surface flat using chemical mechanical planarization (CMP).
Modify	• **Ion Implantation (Implant):** Using intense electrical fields to accelerate ions and penetrate the surface of the wafer, thereby changing the electrical characteristics of the semiconductor material. • **Thermal (Anneals):** Using high temperatures to repair defects in crystal structures or induce phase changes.
Connect	• **Advanced Packaging:** Using front-end wafer fab equipment tools and advanced substrates to connect a variety of chips using increasingly small contacts and wires to increase integration, reduce power and increase performance – of both chips and systems.

PROCESS CONTROL

Analyze	• **Optical Inspection:** Examining wafers at optical resolution to detect the presence of particles and defects between process steps. • **eBeam Defect Review:** Examining suspected defects at electron beam resolution to see and classify defects and root cause process issues. • **eBeam Inspection:** Using electron beam technology to detect and identify defects that cannot be detected by optical inspection. • **eBeam Metrology:** Using electron beam technology to measure critical structures including buried structures with nanometer precision. • **CD-SEM:** Calibrating lithography systems by using electron beam technology to measure the critical dimensions of patterns in photoresist.

"Materials Magic" – Fun Facts

Early ICs only used about 8 elements from the periodic table.
Today, more than 25 elements are combined in 100 different ways using Applied Materials' equipment.

To obtain ultra high film purity, Applied's Endura deposition system can create a vacuum level of 10^{-9} atmospheres.
That's about the same vacuum level at 400km above the earth's surface, or at the orbit of the International Space Station.

To create the transistors on a 300mm wafer, Applied's etch chambers drill a trillion contact holes, each a thousand times finer than a human hair.
That's 10 times the number of stars in the Milky Way.

Applied's CMP systems can smooth the surface of 300mm silicon wafers to a variation of just 5 nanometers.
That's like a lawn mower that can cut every blade of grass on a soccer field to a height that varies by just the width of a human hair.

To create low resistance contacts, Applied's laser anneal system heats the surface of a silicon chip to over 1,000°C in less than a millisecond.
That's approximately the temperature of molten lava.

Applied's wafer inspection systems can find and identify a defect the size of only a few nanometers on a wafer.
That's like spotting a single ant on Earth from outer space, and then identifying its species within seconds.