APPLIED MATERIALS®

MEMORY MASTER CLASS

MAY 5, 2021

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2021 Master Classes

WELCOME

Michael Sullivan

CVP, Head of Investor Relations

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UPCOMING INVESTOR EVENTS

MASTER CLASSES

APRIL 6	May 5	June 16	Second Half 2021
2021 Investor Meeting	Memory	Logic	▪ Specialty semiconductors ▪ Heterogeneous design and advanced packaging ▪ Inspection and process control

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AGENDA

9:00	**PART 1**	HOST: Mike Sullivan Memory Thesis Fireside Chat | Ed Doller
9:15	**PART 2**	HOST: Kevin Moraes, Ph.D. Memory Technology DRAM | Sony Varghese, Ph.D. NAND | Sean Kang, Ph.D.
9:50	**PART 3**	HOST: Raman Achutharaman, Ph.D. Memory Growth Opportunities
10:00	**Q&A**	Raman, Kevin, Mike

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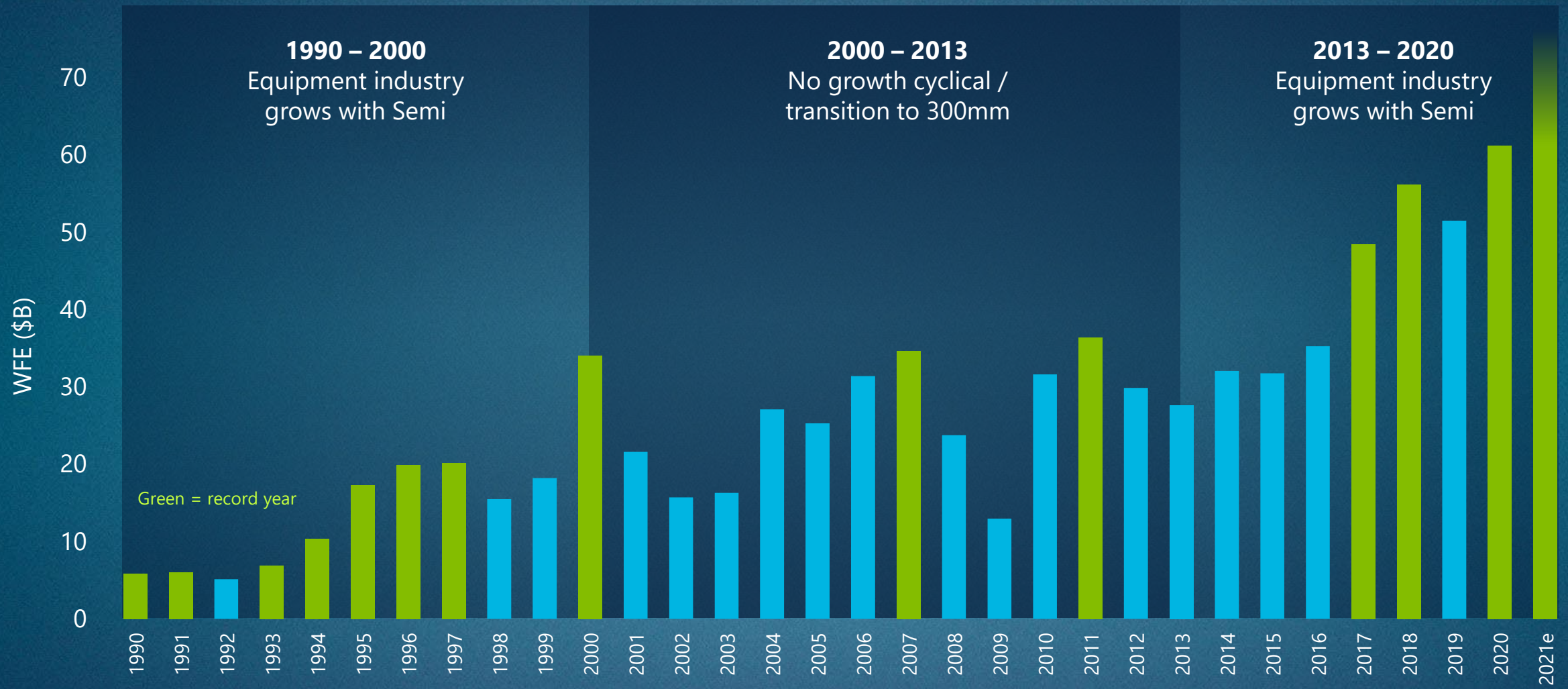
Historical WFE



Source: Gartner, VLSI, Applied Materials.

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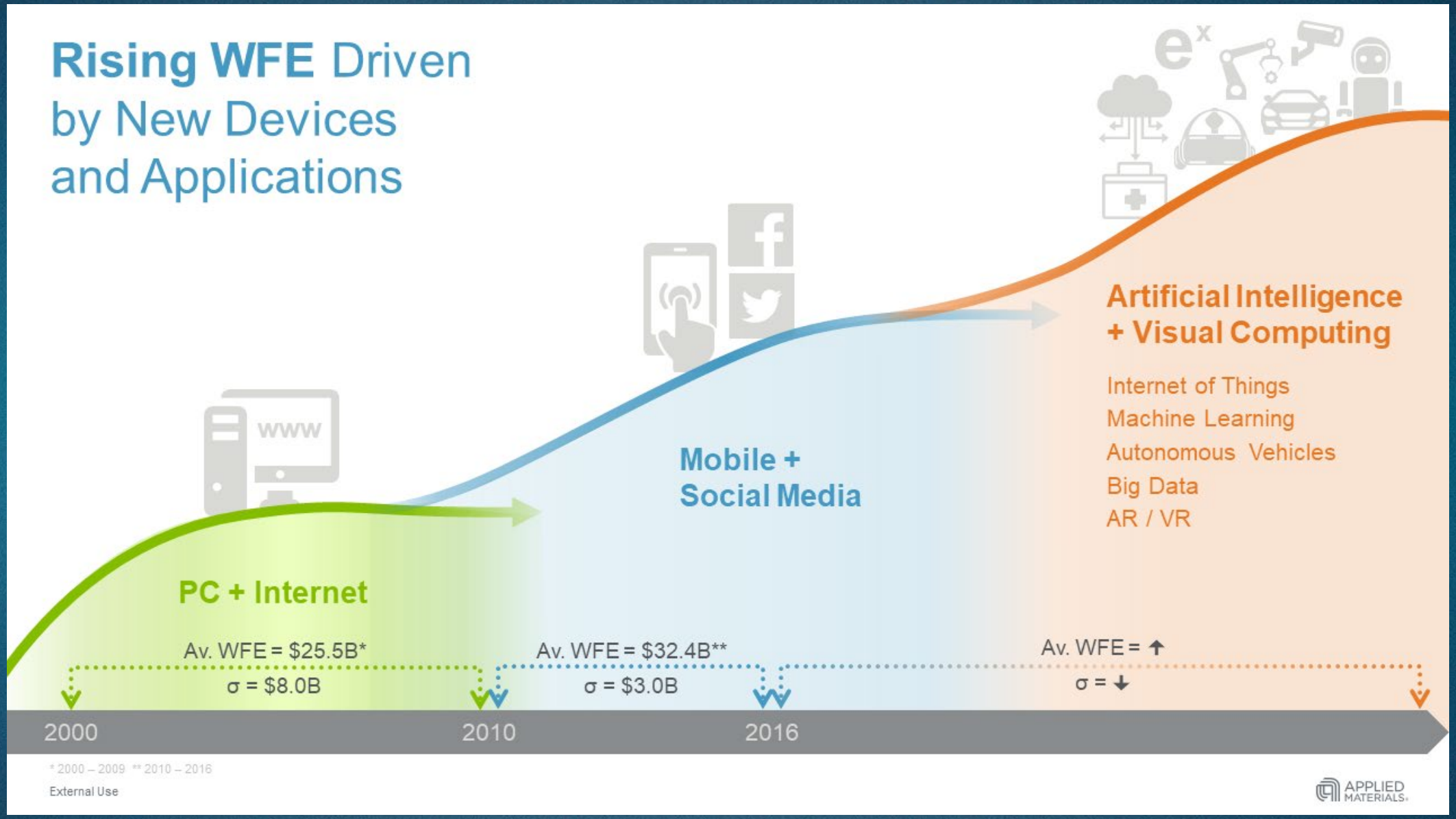
2017 Master Class



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2017 Master Class

Source: The Economist, May 2017

MEMORY DEMAND: CONTEXT

Big Data and Artificial Intelligence can **transform entire industries** – happening faster than many people think

Explosion of data storage requirements created by IoT, Big Data, AI and streaming video has only just begun

Data generation from **new categories can potentially dwarf existing** applications within a few years

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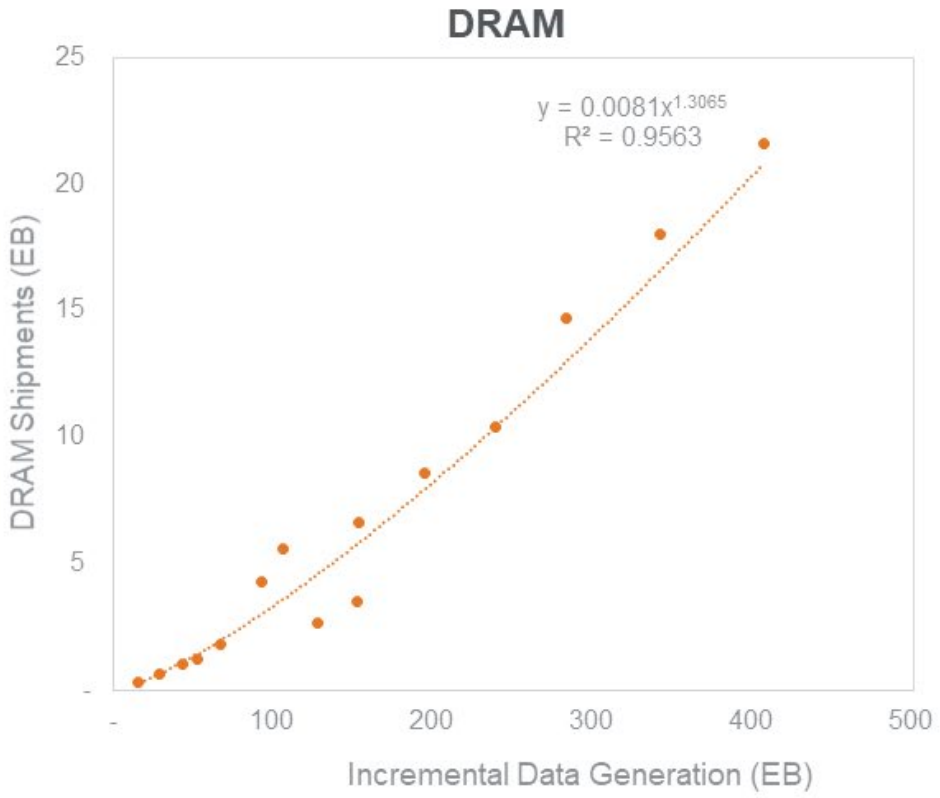
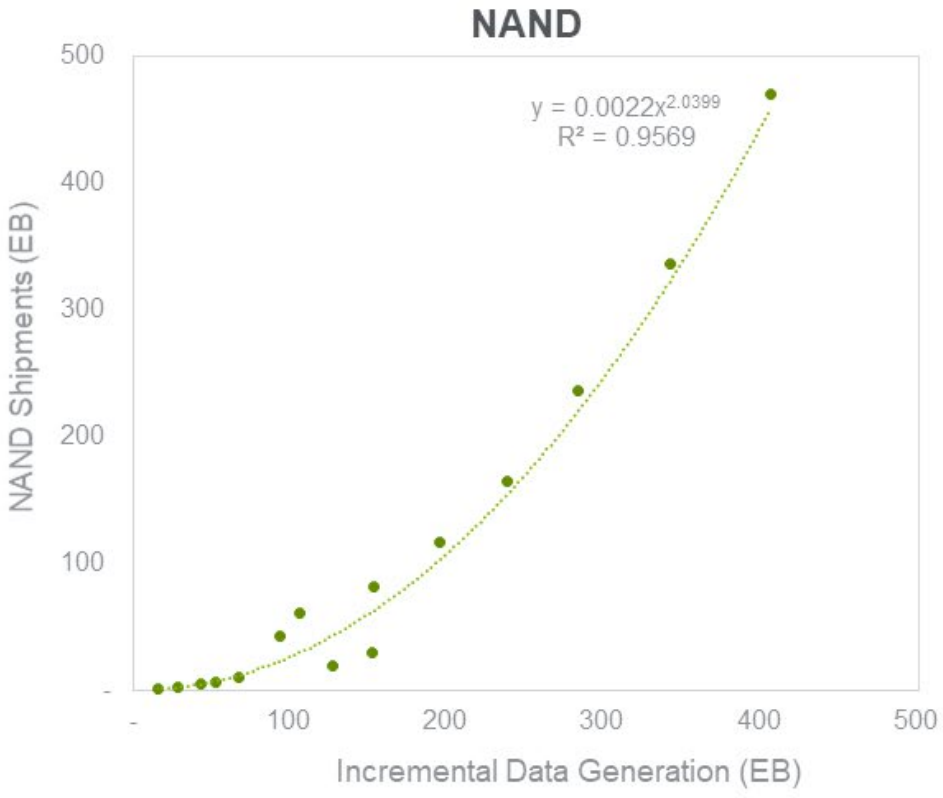
Data Generation to Memory Relationship | Historical





Source: Cisco VNI, Cisco, Gartner, Factset, Applied Materials internal analysis
2006 to 2016 data from Cisco and Gartner. 2017 to 2020 projections from Cisco for data generation (VNI IP traffic), and industry average estimates for DRAM and NAND content shipments

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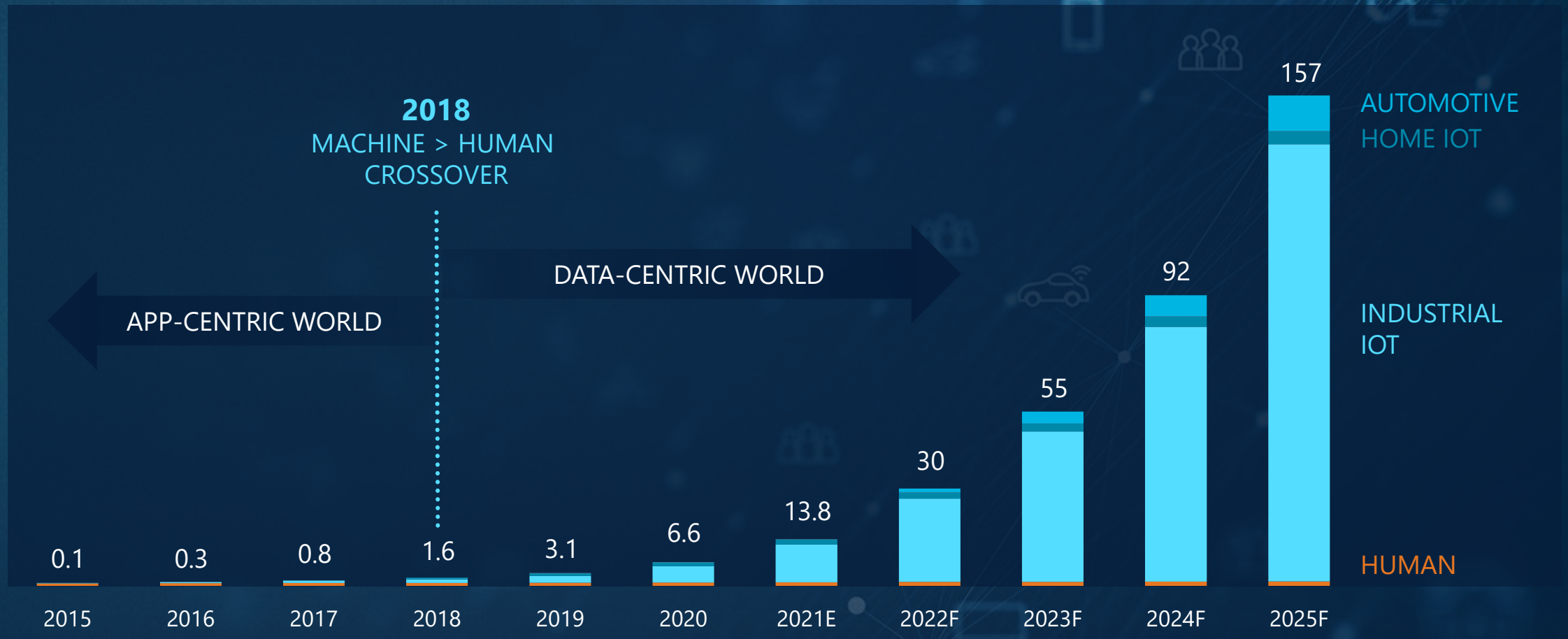
Data Generation By Category (ZB)



SEMI GROWTH NO LONGER LIMITED BY HUMAN CONSUMPTION

Source: Applied Materials

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Semi content per unit	2015	2020	2025F
HIGH END SMARTPHONE	$100	$170	$275
AUTO (GLOBAL AVERAGE)	$310	$460	$690
DATACENTER SERVER (CPU + ACCELERATOR)	$1,620	$2,810	$5,600
SMARTHOME (GLOBAL AVERAGE)	$2	$4	$9

SILICON CONTENT GROWING AS EVERYTHING GETS SMARTER

Source: Applied Materials

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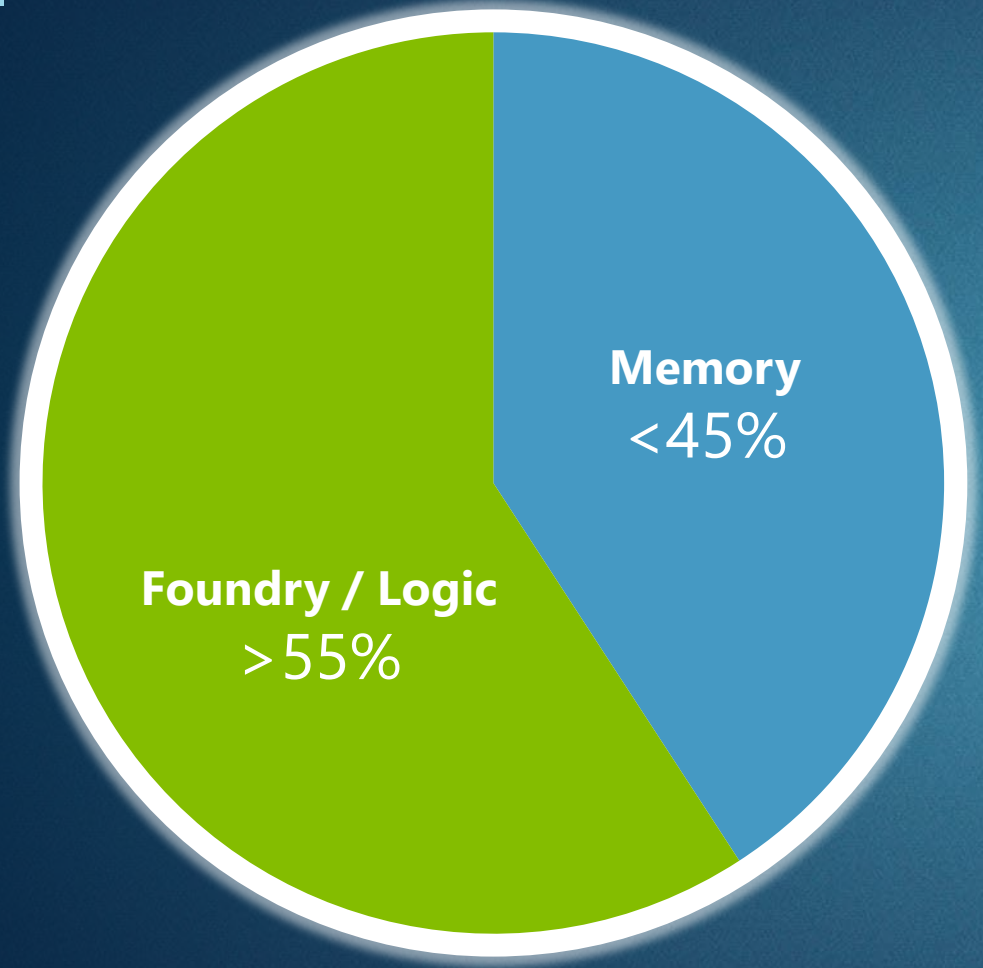
Historical WFE Mix



Long-Term Average

Foundry / Logic vs. Memory mix consistent over time

- 10-year and 20-year averages: Foundry / Logic >55%
- Foundry / Logic > Memory in 17 of past 20 years

Source: Gartner, VLSI, Applied Materials

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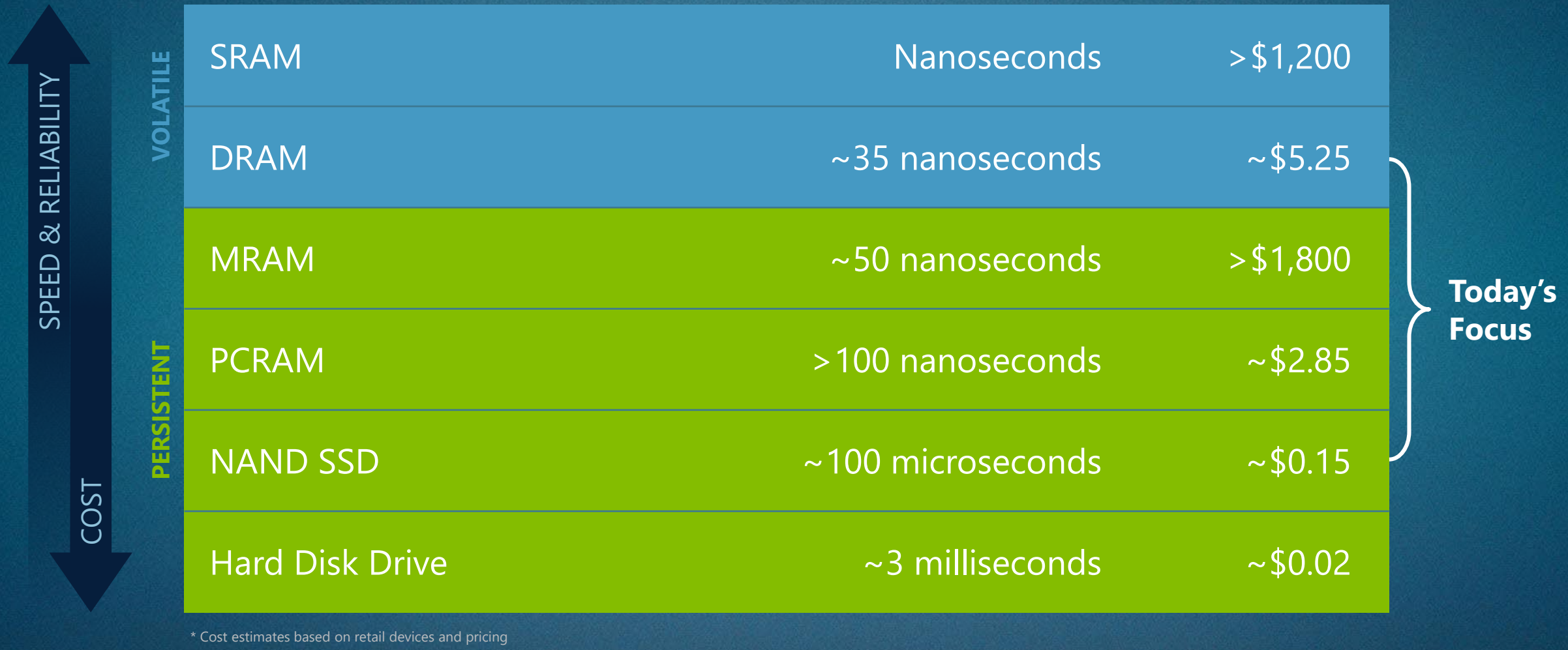
Memory Market Segmentation



* Cost estimates based on retail devices and pricing

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PART 2

Memory Challenges and Roadmaps – DRAM

Sony Varghese, Ph.D.
Director, Strategic Marketing

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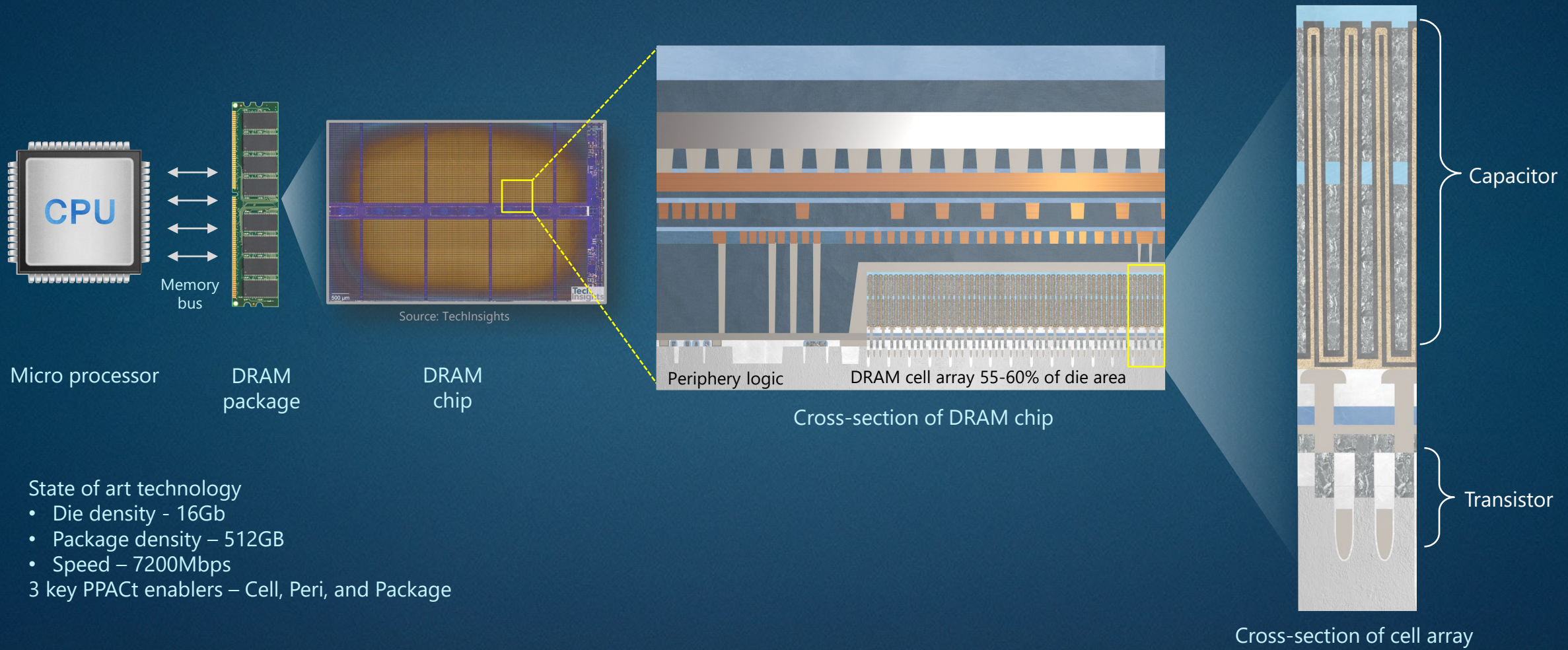
DRAM: High-Speed Volatile Memory



State of art technology
- Die density - 16Gb
- Package density – 512GB
- Speed – 7200Mbps

3 key PPACt enablers – Cell, Peri, and Package

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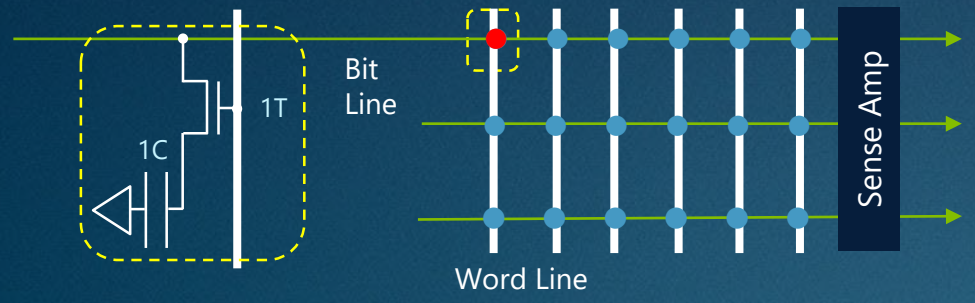
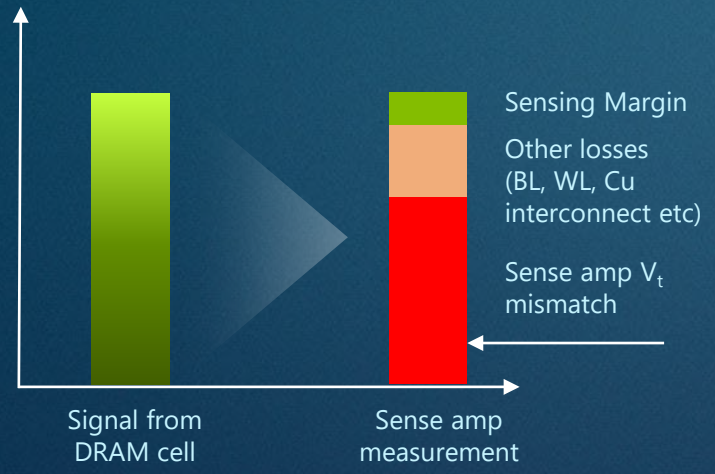
Physics of DRAM and Implications for Scaling

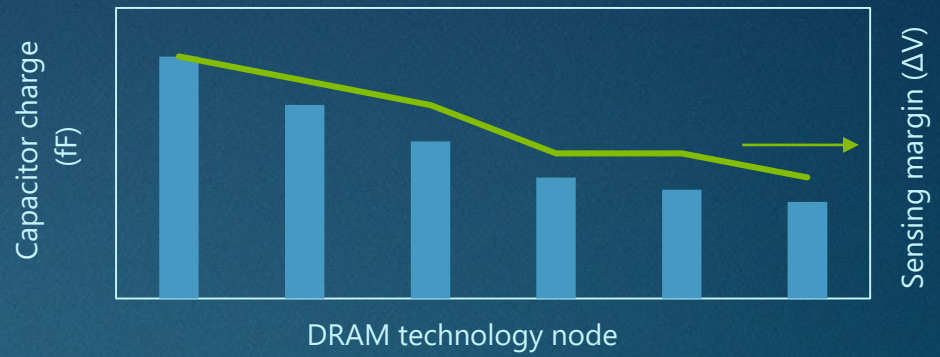
DRAM read operation schematic



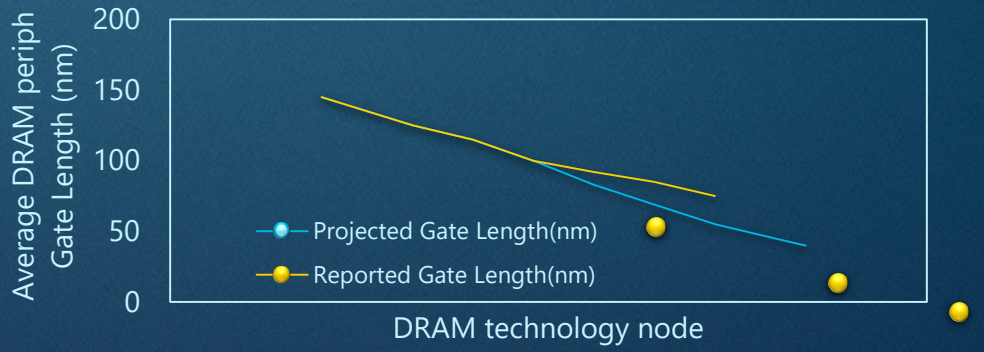


Peri transistor variability (V_t mismatch) impacts sensing margin

Sensing margin[1] is shrinking with decreasing capacitor charge



Gate length scaling[2] lagging projection for acceptable sensing margin



Source 1: A. Spessot, IEEE Transactions on electron devices, vol. 67, no. 4, April 2020
Source 2: TechInsights and Applied Materials projections

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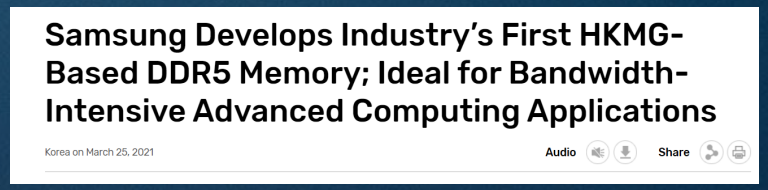
DRAM Scaling Roadmap

Year of first production	Node (nm)	Cell capacitance (fF)	Periphery gate length (nm)	Key inflections
2017	20	13	100-115	Lattice for capacitor
2019 ~	17	10	75-90	SAQP[1]
2021 ~	15	7	65-80	DDR5, More SAQP, EUV, HKMG[2]
2023 ~	13	5	50-60	Commodity DRAM HKMG[2]
2025 ~	11	3	45-55	Low resistance metal
2025 +	3D DRAM	4+	New CMOS	Layered high mobility channel[3]



1. SAQP – Self Aligned Quadruple Patterning
2. HKMG – High k Metal Gate
3. 15X higher mobility than 3DNAND Channel

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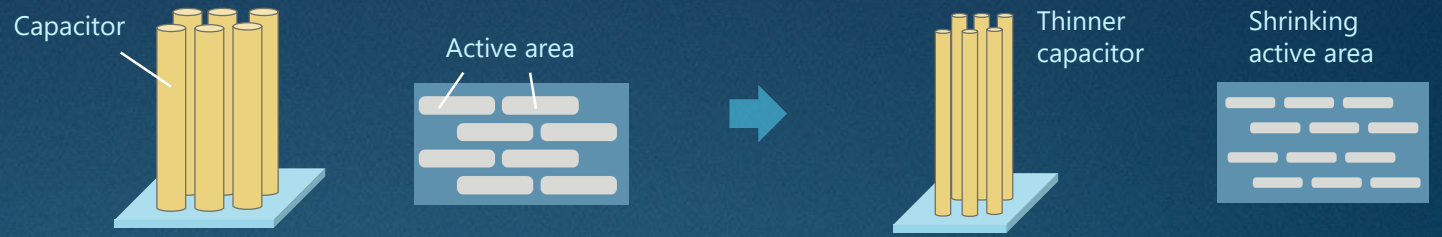
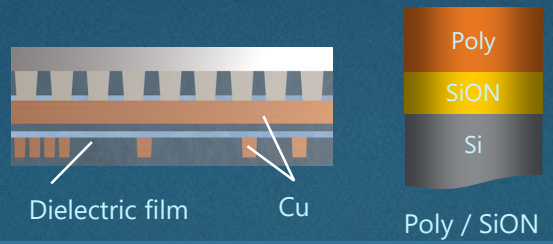
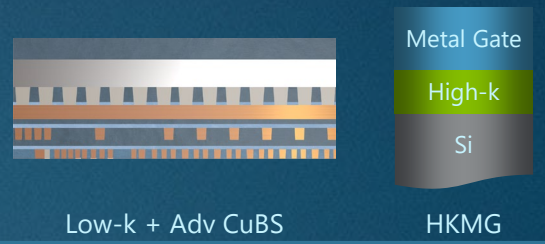
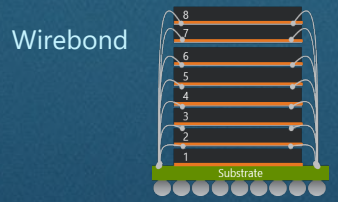
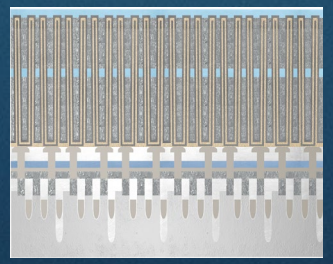
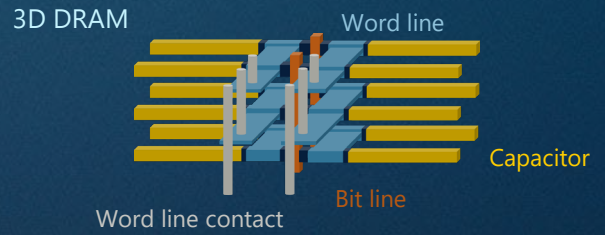
Levers for DRAM Scaling

Scaling lever	Key modules	Current	Inflections
Cell	Capacitor Active silicon area Word line / bit line		
Periphery	Interconnect Transistor		
3D stacking	Bond pad Thru silicon via (TSV) Bump		
New architecture	High mobility channel Conductor etch Selective removal HAR gapfill Advanced doping		

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Levers for DRAM Scaling: Cell Region

Scaling lever	Current	Inflections
Cell region		

Module	High Value Problems	Solutions
Capacitor	High aspect ratio capacitor fabrication Higher etch profile variability and defects	New hardmask materials Co-optimized etch technology with metrology feedback
Active silicon area	Shrinking Si active area Reduced drive current and increased variability	Patterning SAQP or EUV with HAR Etch Low Si loss from oxidation, Low damage from implant

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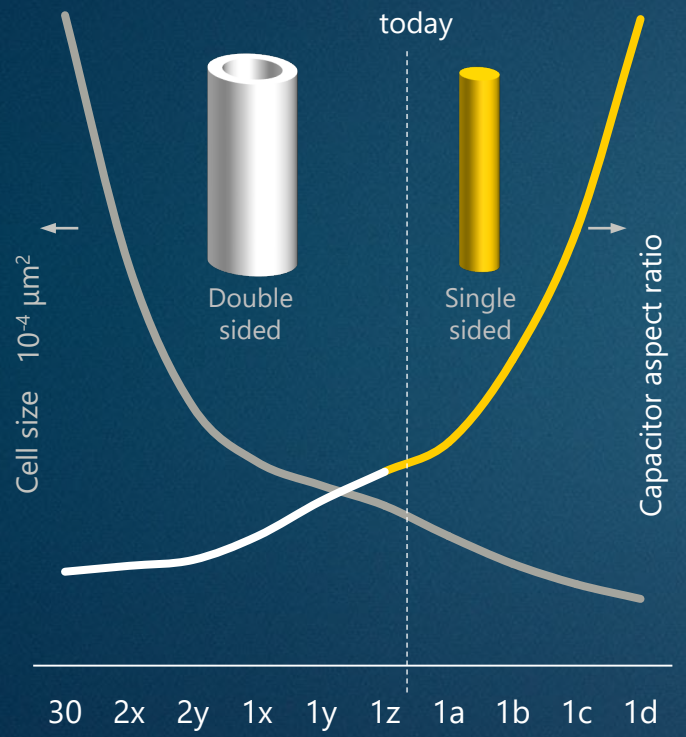
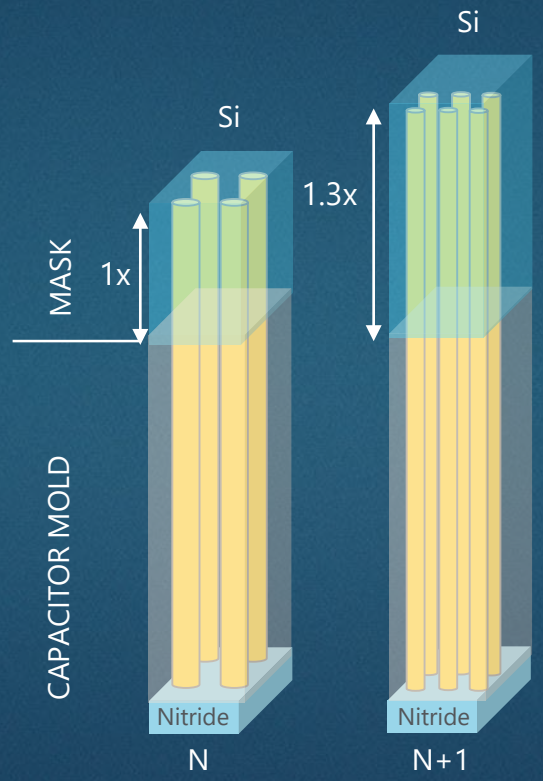
DRAM Capacitor Scaling Challenges

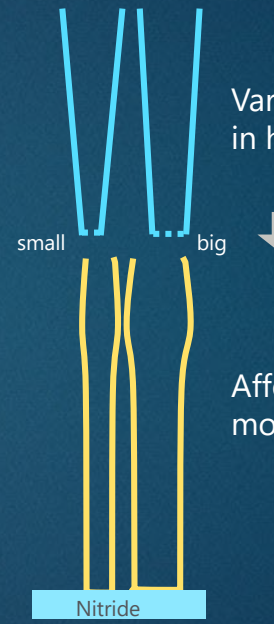
Shrink + geometry change = High AR



Need taller mask for patterning

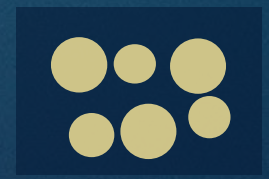


Higher etch variability and defects



Varying hole sizes in hard mask

Affects circularity of mold profile



Local CD variation
- Unopened holes
- Bridging / shorts

AR = Aspect Ratio

CD = Critical Dimension

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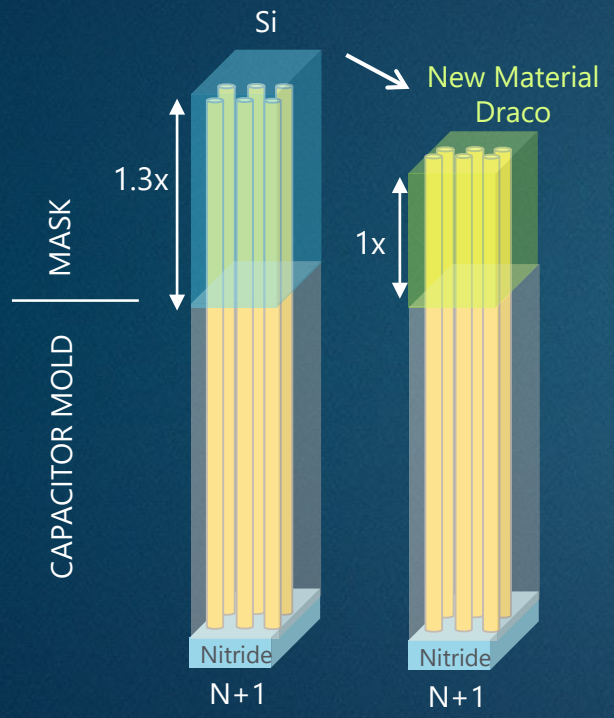
Innovations to Enable Low Variability High AR Etch Process

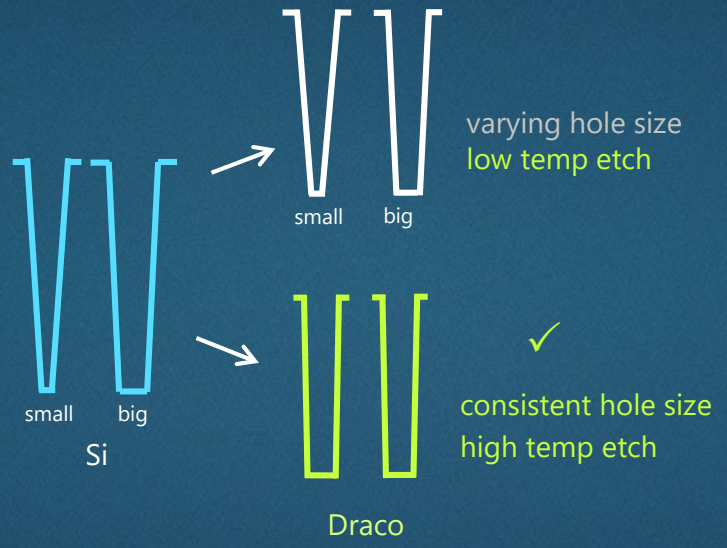
Draco™: New hard mask material
(Higher modulus and selectivity)



Tunable film properties for selectivity
Unique precursor chemistry

+

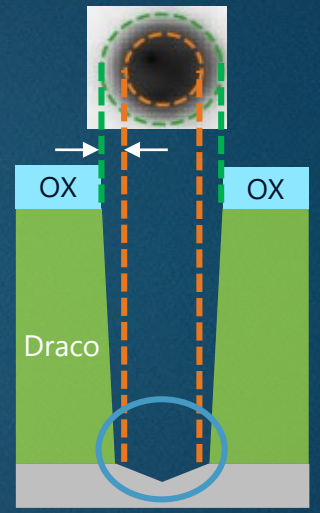
New high temp etch technology
(Better profile and CD uniformity)



Industry leading >200°C capability
Higher conductance Sym3® design

+

Unique metrology
(Faster and better sampling error)



Non-destructive, bottom imaging with actionable measurements

* CD = Critical Dimension

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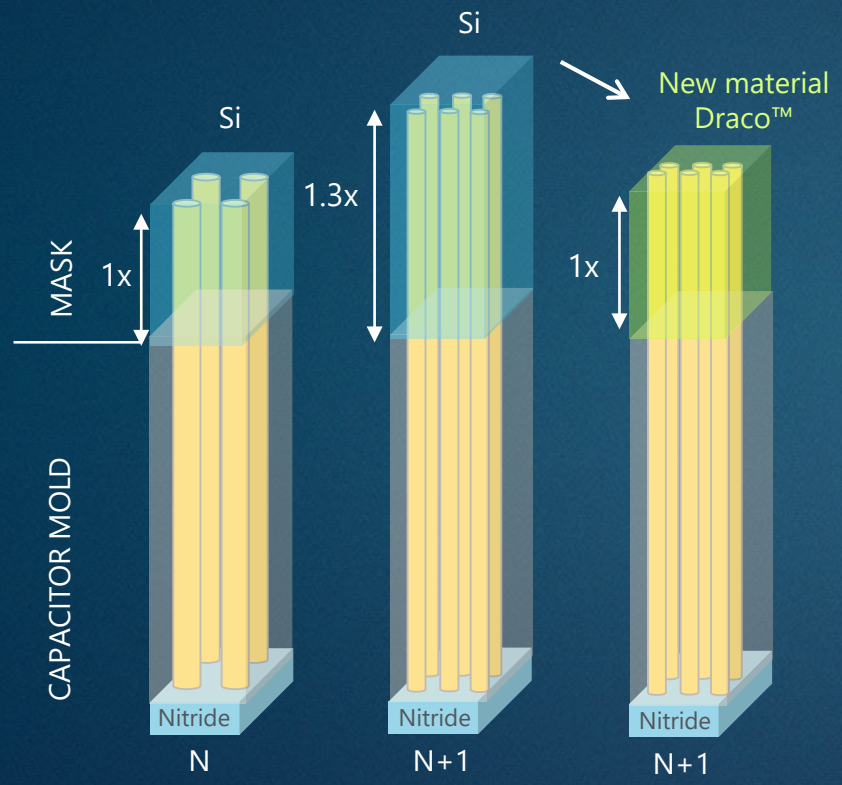
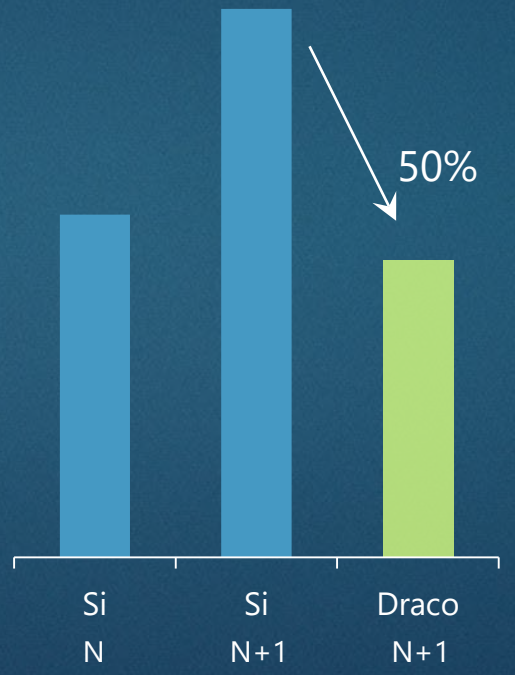
Variability and Defect Reduction with Co-Optimization

Thinner mask with lower AR + New etch

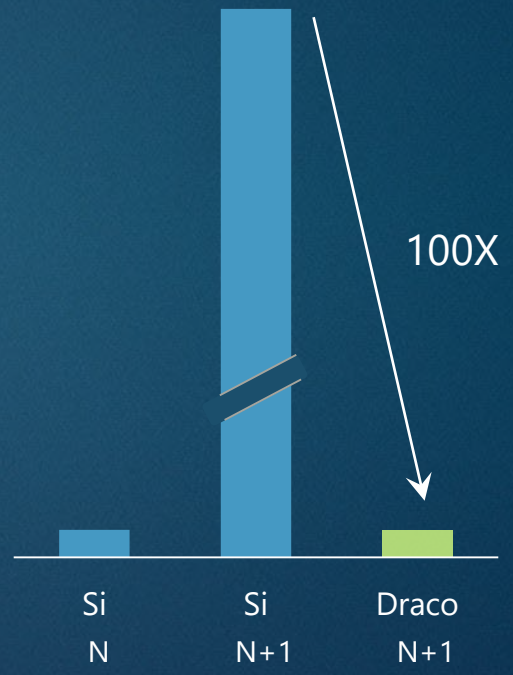


Enabling improved CD uniformity and defect performance

Local CD uniformity improved



Bridging defects substantially reduced



AR = Aspect Ratio
CD = Critical Dimension

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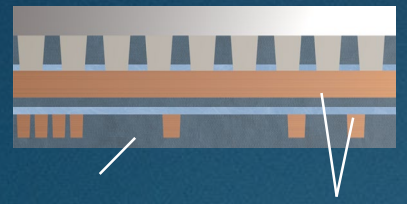
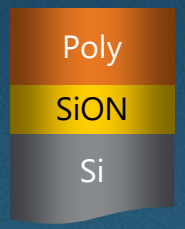
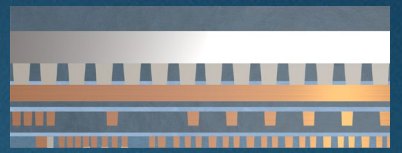
Levers for DRAM Scaling: Periphery Region

Scaling lever	Current	Inflections
Periphery	 TEOS dielectric Cu  Poly / SiON	 Low-k + Adv CuBS  HKMG

Module	High Value Problems	Solutions
Transistor	V_t variability High gate leakage current	New materials (Metal Gate, Dipole) Interface engineering (High-k, Inter Layer, Channel)
Interconnect	Power loss and RC delays with narrow pitch Early device failure from electromigration	Low capacitance dielectric Advanced copper interconnect

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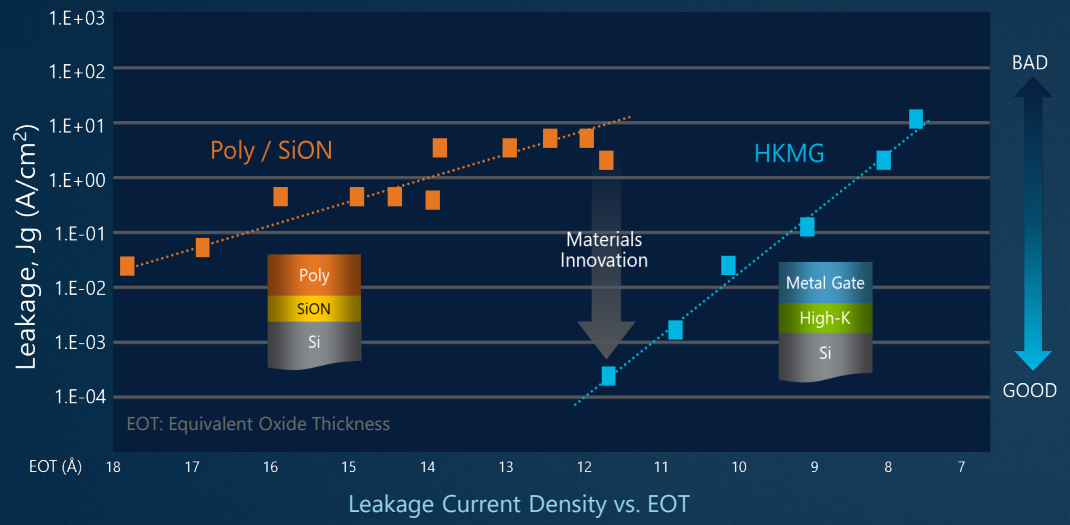
PPACt Scaling of DRAM Peri Transistors with HKMG

HIGH VALUE PROBLEM

Thinner insulation layer = higher leakage



Leakage Current Density vs. EOT

REQUIREMENTS

Multiple new materials

6-7 materials stack
High complexity

Interfaces very critical

How we treat
How we terminate

APPLIED LEADERSHIP PRODUCTS

Metal gate
Dipole for Vt engineering
PMOS channel

High-k film treatments
Interlayer/HK interface
Interlayer Engineering
Channel interface

PPACt gains with HKMG*

13% lower power
2X speed

Source: Samsung newsroom, Mar 25, 2021

Accelerating adoption of Logic-like process innovations in DRAM

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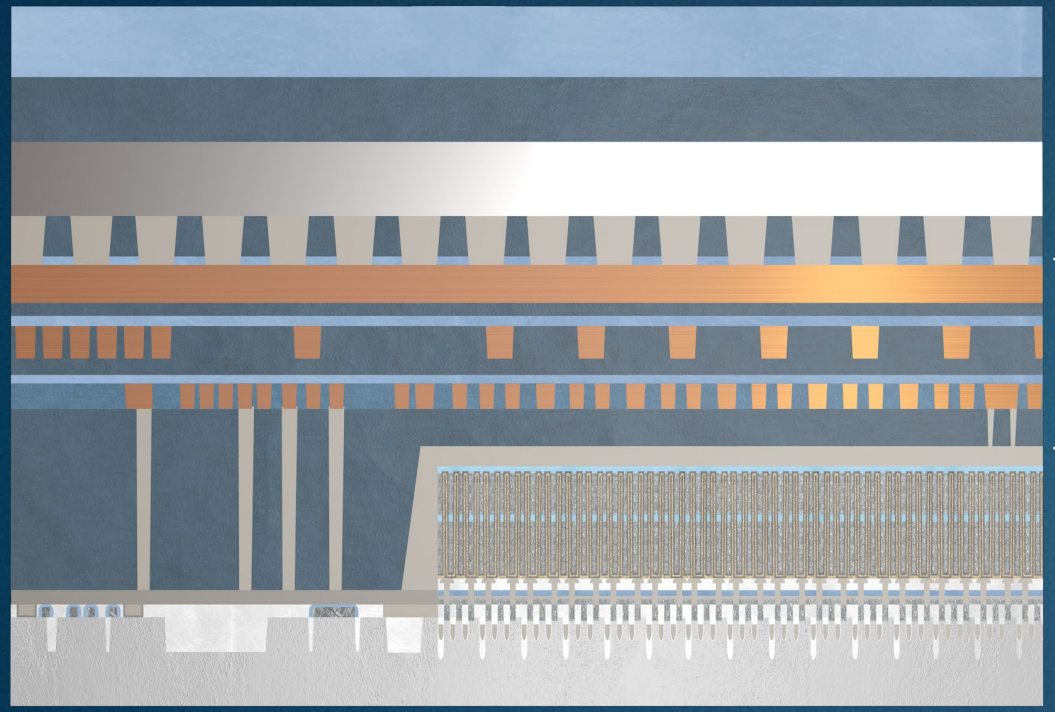
DRAM Periphery: Interconnect Scaling



- *ρ Conductor Resistivity*
- *k, Effective Dielectric Constant (Low k)*
- *ε_0 Permittivity in Vacuum*
- *L Interconnect Length*
- *w_m Metal Width*
- *w_d Metal Spacing*

- *C Capacitance*
- *V Voltage*
- *F Frequency*

HIGH VALUE PROBLEM

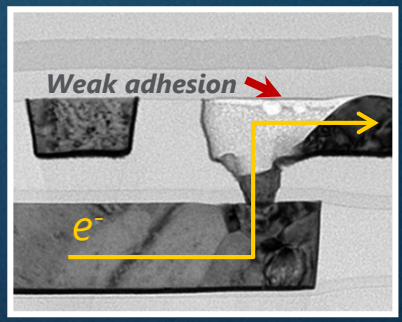
Periphery scaling reduces wire pitch (w_d) and copper line widths (w_m)

At reduced pitch, signal delay and power losses increase

$$\text{RC Delay} = \rho k, \varepsilon_0 \frac{L^2}{w_m w_d}$$

$$\text{Power} = CV^2F$$

Higher current density in narrow lines, cause early electromigration failures



Source: Applied Materials

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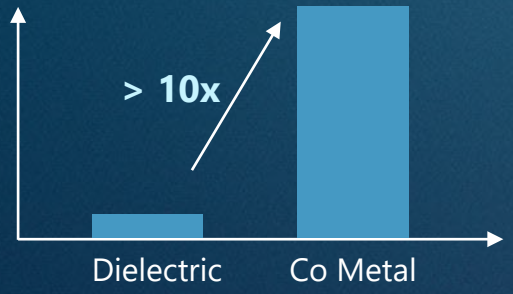
DRAM Adopting Interconnect Innovations from Logic

Technology solutions

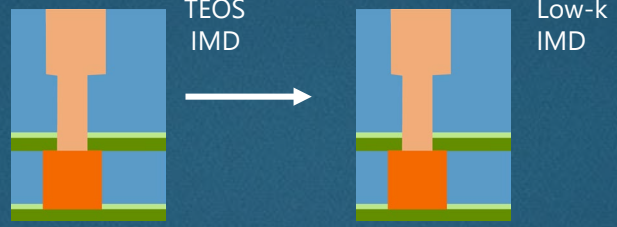
Dielectric constant

Electromigration lifetime



Adoption of low-k

TEOS silicon oxide → low-k



D1X
0 steps

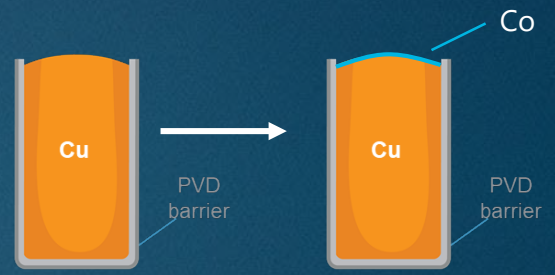
D1A
3 steps

Producer® Black Diamond®
Industry leading low-k material

+

Adoption of Cobalt capping

Cu interconnect + Co capping



D1Z
3 steps

D1B
4 steps

Endura® CuBS + CVD Cobalt
Industry leading interconnect technology

IMD: Inter-Metal Dielectric

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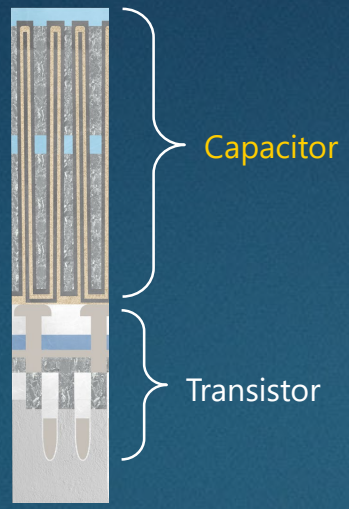
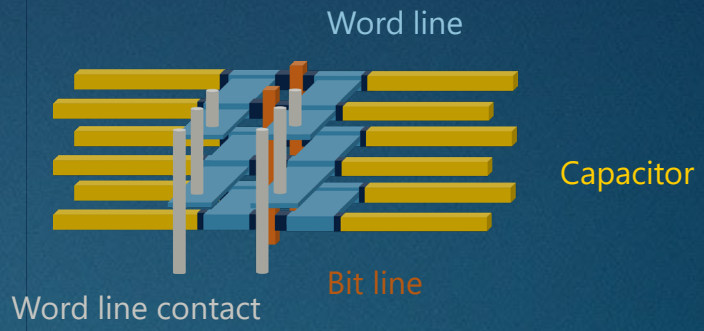
Levers for DRAM Scaling: New Architecture

Scaling lever	Today	Roadmap
New architecture	Planar DRAM 	3D DRAM 

Module	High Value Problems	Solutions
3D DRAM	Patterning costs challenges Inadequate sensing margin	High mobility channel EPI /PVD/ALD Conductor etch HAR gap fill Selective removal Advanced doping

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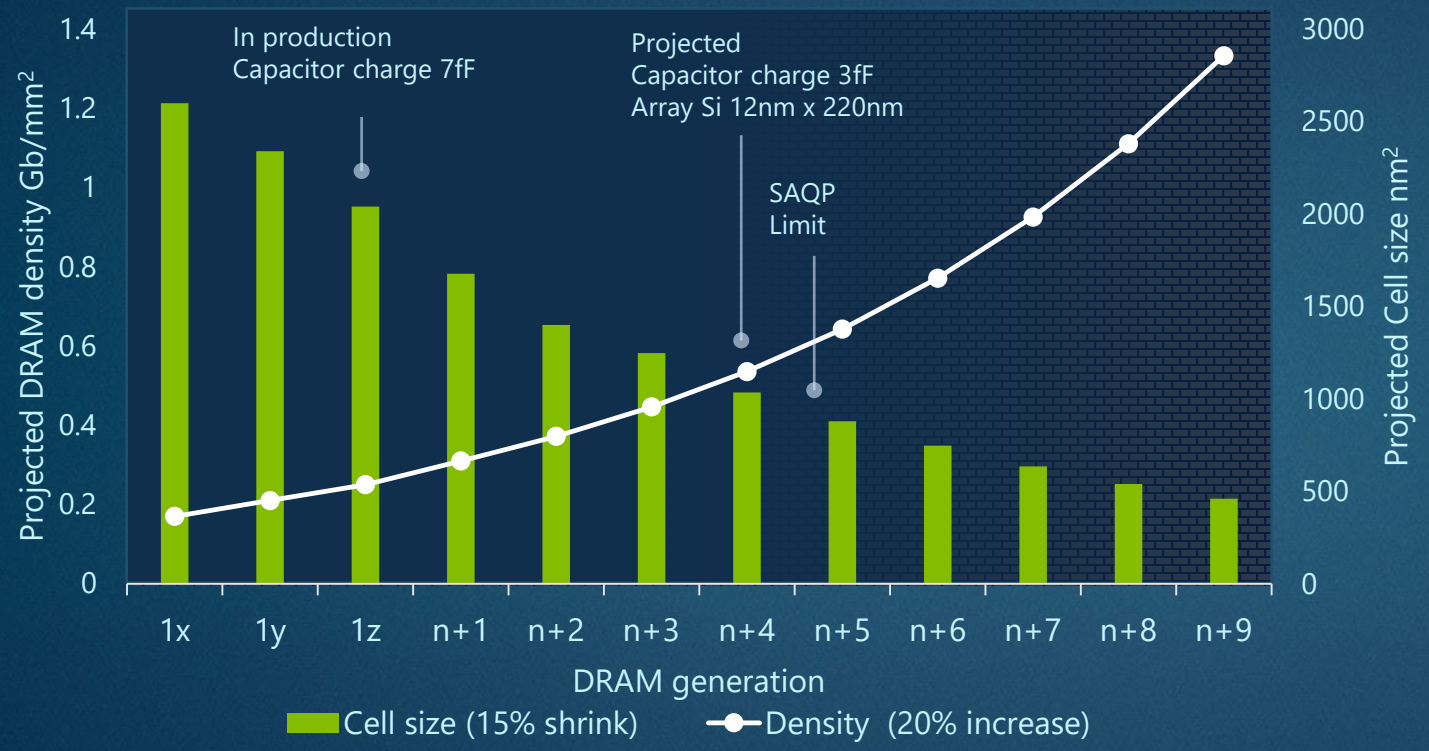
Planar DRAM Scaling Limitations



Industry targets 20% density increase per node

SAQP limit beyond n+4

Cost challenges from patterning may make scaling uneconomical

Reduction in capacitor charge → inadequate sensing margin

New methods to scale are needed to meet PPAC

Applied Materials Projections based on IRDS DRAM roadmap

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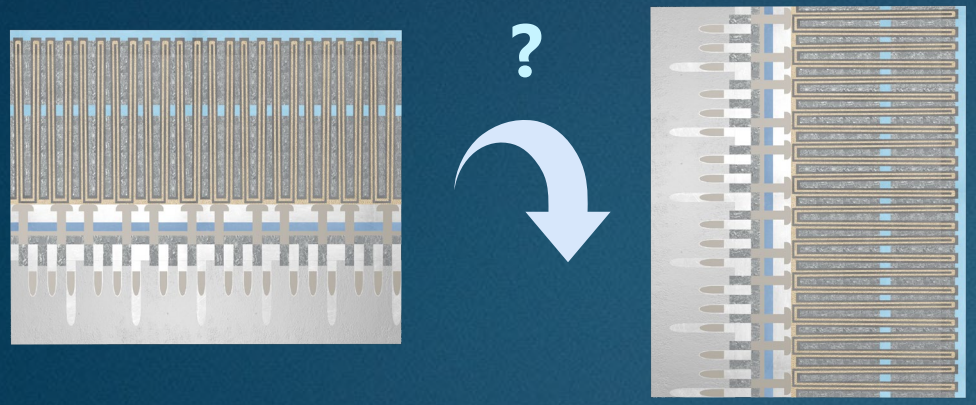
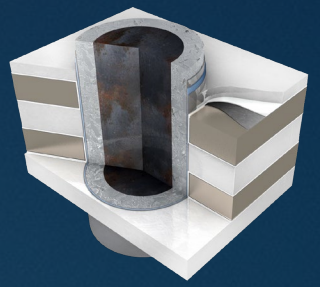
Will 3D DRAM be Fabricated Like 3D NAND?

Can DRAM scale by stacking 1 cell over the other?
It worked for NAND



DRAM must operate **1000X** faster than NAND
Requirements more similar to logic Gate-All-Around (GAA)

	NAND cell	DRAM cell
		
Write speed	50,000 ns	10 ns
Endurance	1e4 cycles	1e18 cycles
Channel mobility	Low (poly Si)	High (Si)
Storage discharge	Slow (charge trap)	Quick (capacitor)

New material innovations required to enable higher mobility, ultra-low defect channels for 3D DRAM

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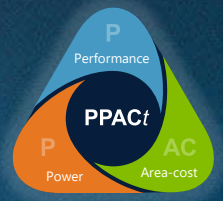
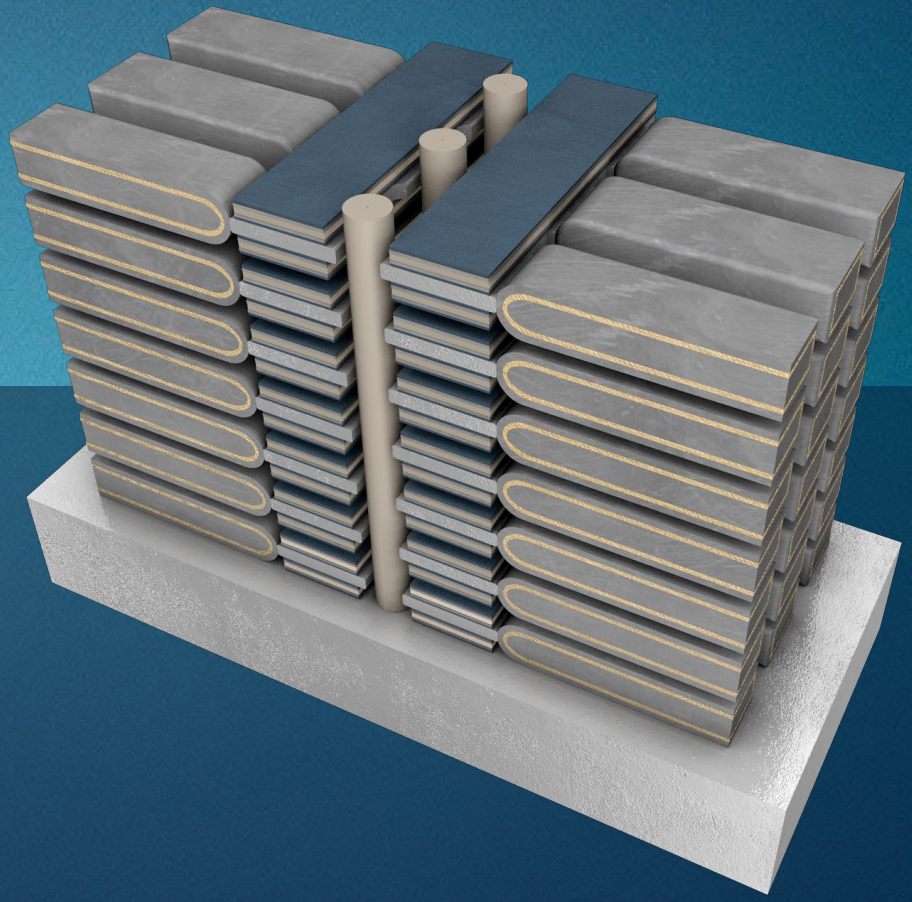
Enabling the Roadmap to 3D DRAM PPACt Scaling



Unit Process Leadership

- High mobility channel Epi /PVD/ALD
- Conductor etch
- HAR gapfill
- Selective removal
- Advanced doping

+ Integrated Materials Solutions Leadership



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Enabling PPACt Roadmap for DRAM

DDR4, 1.2V | **DDR5,** 1.1V | **DDR6**

2.3Gbps 8Gb	2.6Gbps 8Gb	3.2Gbps 8Gb	4.8Gbps 16Gb	5.6Gbps 16Gb	7.2Gbps 16/32Gb	12Gbps* 32Gb
2015	2017	2019	2021		2023	2025

SAQP

Low Damage Implant

HKMG

3D DRAM

EUV

Dual deck capacitor

Low K

Capacitor Hardmask

Co Capping

Low R Metals

Well positioned with leadership products and integrated materials solutions

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make possible

PART 2

Memory Challenges and Roadmaps – 3D NAND

Sean Kang, Ph.D.
Sr. Director

MEMORY MASTER CLASS | May 5, 2021

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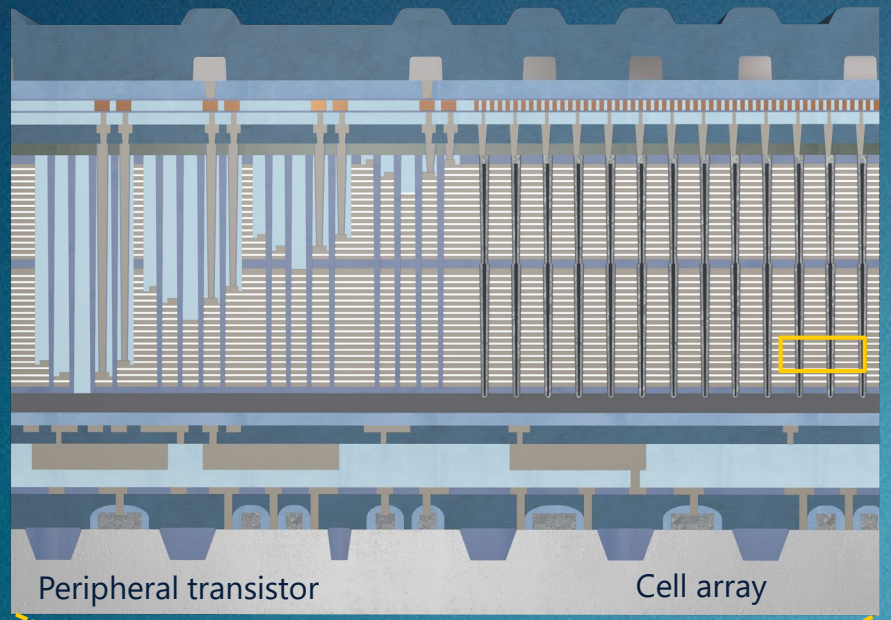
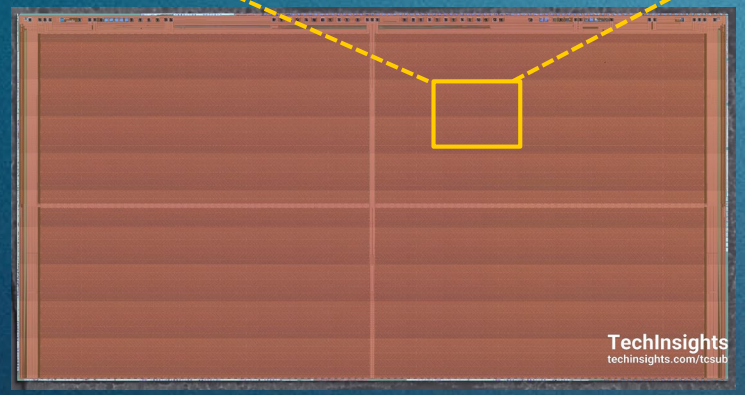
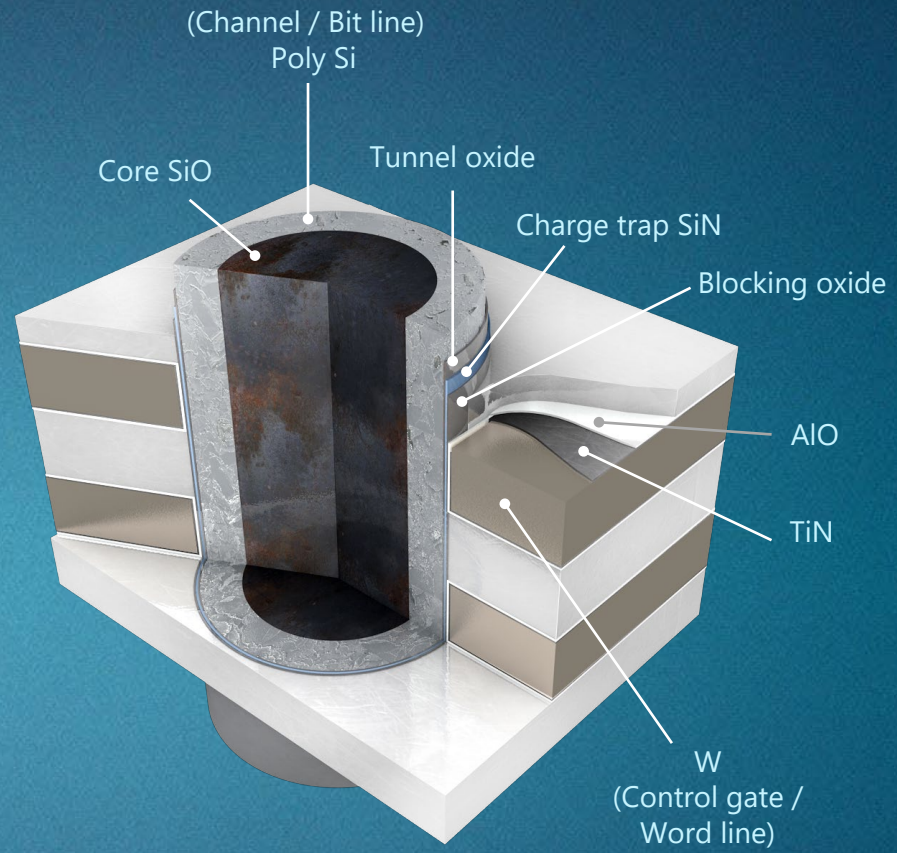
3D NAND: A High-Density Storage Memory





Source: TechInsights



State of the art technology:

- Die density: 1Tb
- Number of layers: 176pairs
- Maximum IO speed: 1.6Gbps
- Bit/cell: QLC

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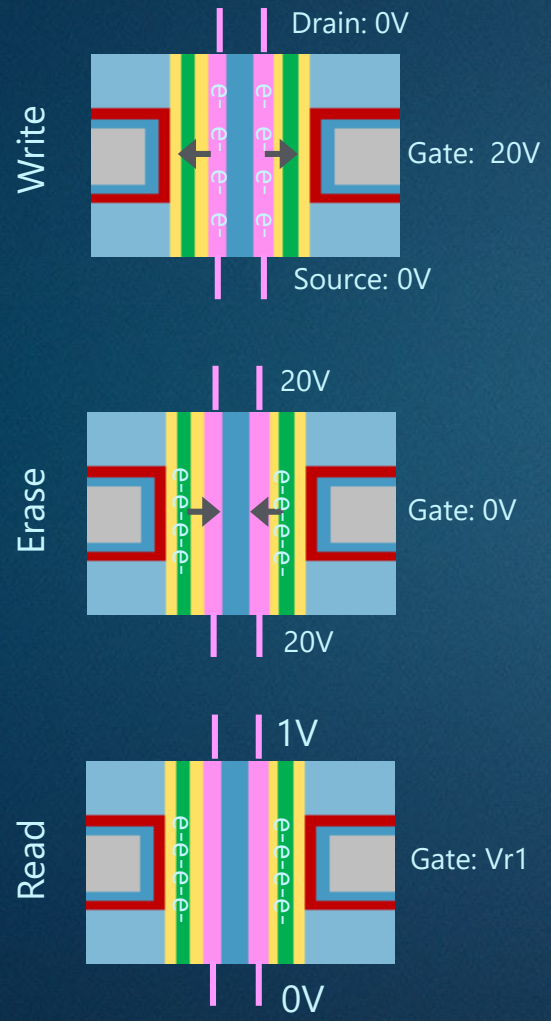
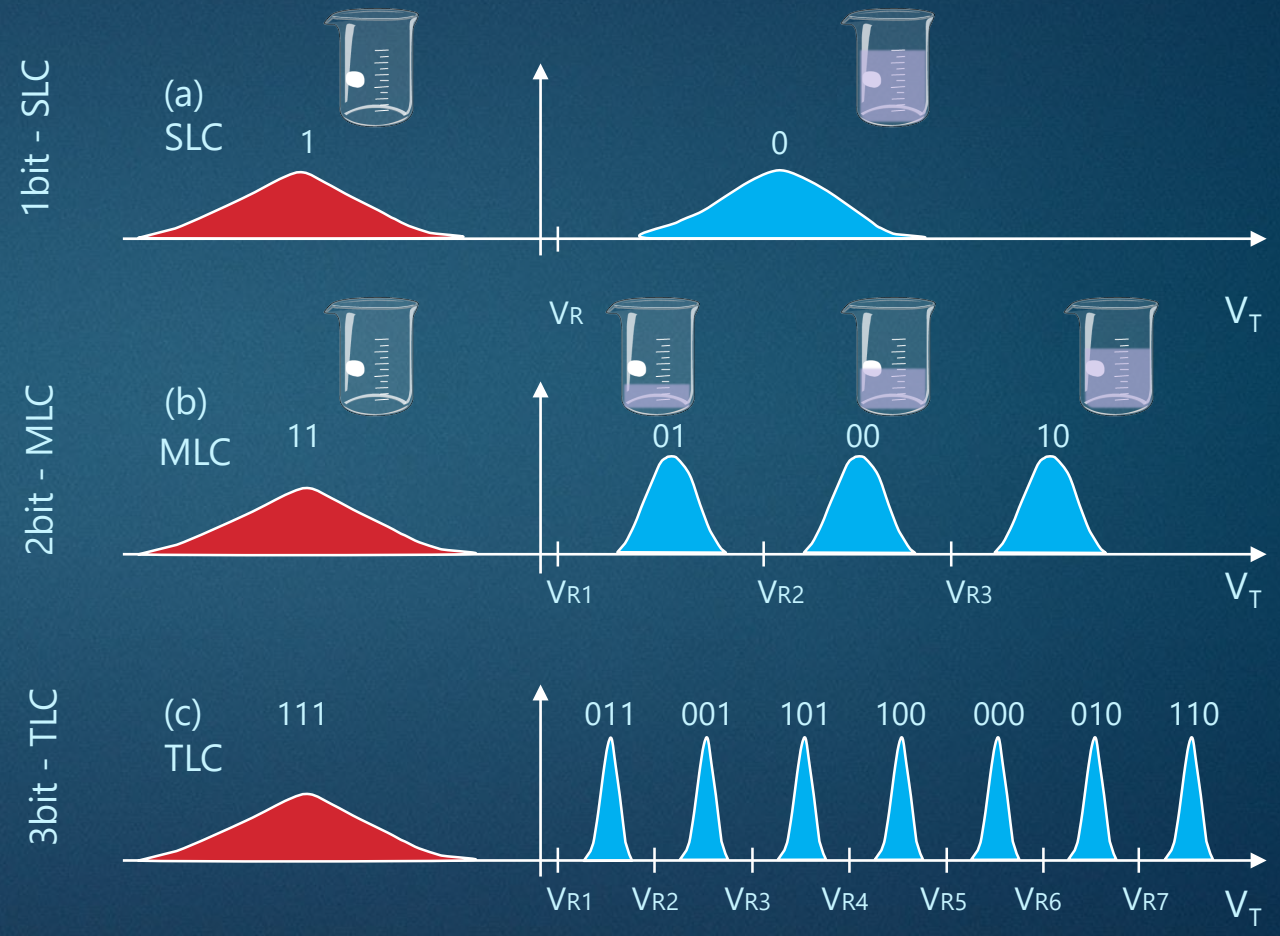
Physics of 3D NAND and Implications for Scaling

How 3D NAND works



Bits Scaling



Vol. 105, No. 9, September 2017 | Proceedings of the IEEE 1609

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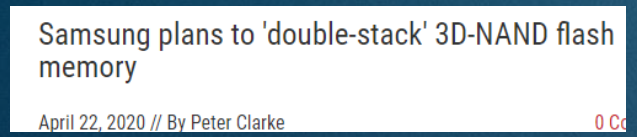
3D NAND Scaling Roadmap

Year of first production	Node (pair)	Stack height (µm)	Pair thickness (nm)	Key structure inflections
2015	~30	~2.5	~70	
2017	~70	~5	~60	
2019 ~	>100	~7	~50	Staircase Opt.[1]
2021 ~	>150	~ 8.5	45 ~ 50	2 Tier, CuA[2]
2023 ~	>250	>10	40 ~ 45	Cell Design[3]
2025 ~	>350	>> 10	~40	>2 Tier, CoA[4]


Samsung plans to 'double-stack' 3D-NAND flash memory

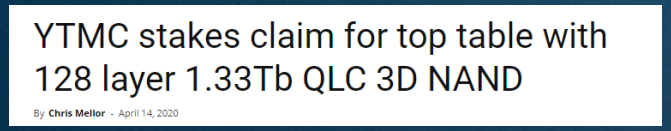
April 22, 2020 // By Peter Clarke


SK hynix Unveils the Industry's Most Multilayered 176-Layer 4D NAND Flash

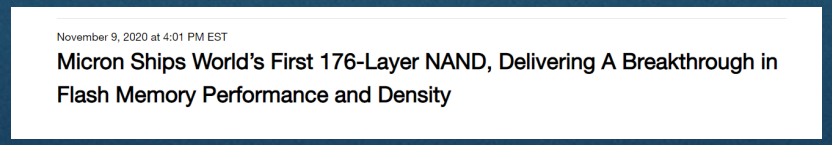
December 4, 2020


Dec 16, 2020, 09:00am EST | 1,316 views

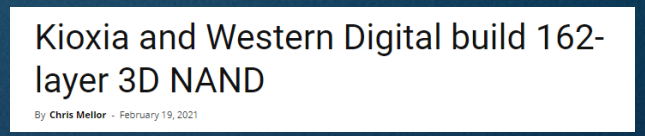
Intel's New Optane And 144-Layer NAND SSDs Enable PCs As Well As Data Centers


YTMC stakes claim for top table with 128 layer 1.33Tb QLC 3D NAND

By Chris Mellor - April 14, 2020


November 9, 2020 at 4:01 PM EST

Micron Ships World's First 176-Layer NAND, Delivering A Breakthrough in Flash Memory Performance and Density


Kioxia and Western Digital build 162-layer 3D NAND

By Chris Mellor - February 19, 2021

1. Staircase optimization for area saving
2. CuA: CMOS Under Array
3. Cell layout intensification
4. CoA: CMOS over Array

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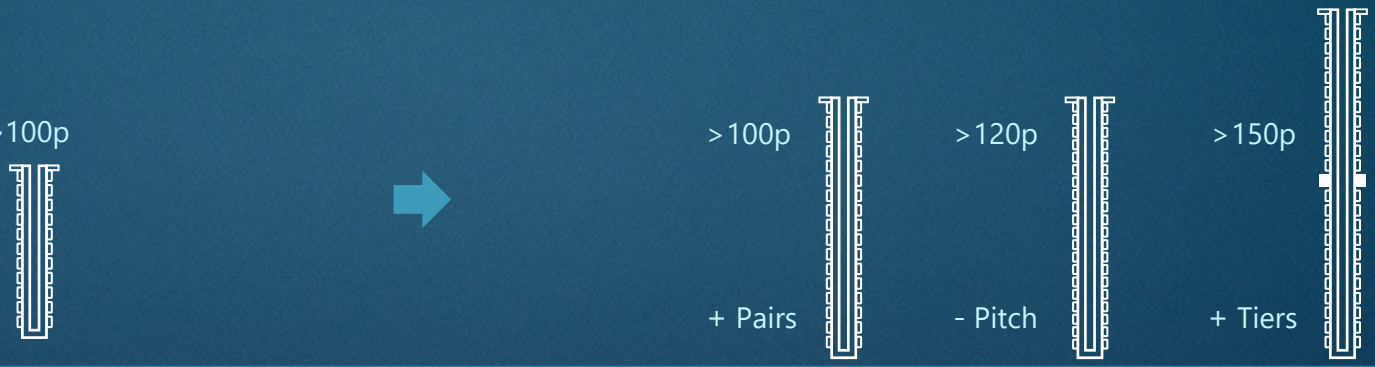
Three Levers for 3D NAND Scaling

Scaling lever	Current	Inflections
Lateral	Staircase; CMOS near Array; Memory Holes; Slit	Zig-zag staircase; CMOS under Array; CMOS over Array; + Holes
Vertical	~100p	>100p + Pairs; >120p - Pitch; >150p + Tiers
Bits per cell	3b/c 8 states	4b/c 16 states



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Levers for 3D NAND Scaling: Lateral

Scaling lever	Current	Inflections
Lateral		

Module	High Value Problems	Solutions
Staircase	Single flight not scalable Consumes 1-2% die	Zig-zag staircase architecture Multi-pair etch and large HAR gap fill
CMOS	CMOS near array consumes 30% of die CuA: Transistor higher thermal budget CoA: W2W bonding	Architecture change, CuA or CoA CuA: Optimized ion implant and annealing CoA: Low dishing CMP and heterogeneous bonding
Memory array	Memory hole density Slits consume >10% of array (holes + slits)	SiN exhume and ALD

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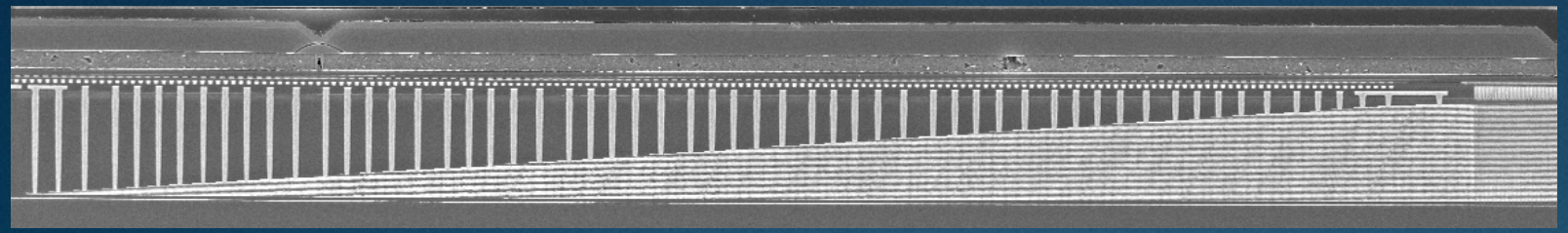
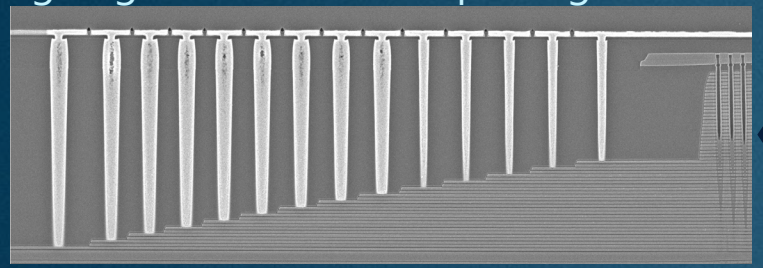
3D NAND Staircase Area Savings

Traditional Staircase – Single Flight



48 Pairs
~ 60 um long

Zig-zag Staircase – Multiple Flights



Traditional staircase est: ~120um
~ 90% Staircase Area Savings

96 Pairs
~10 um long

Limitations	Traditional staircase has area penalty, not scalable to more pairs
New Capabilities	Zig-zag Staircase brings new challenges in profile control, CD/ER uniformity, throughput and cost
Adoption	3 in production, others in R&D

Continuing leadership position with Sym3 etch

Cross-section Images from TechInsights
CD: Critical Dimension
ER: Etch Rate

Applied Materials External Use

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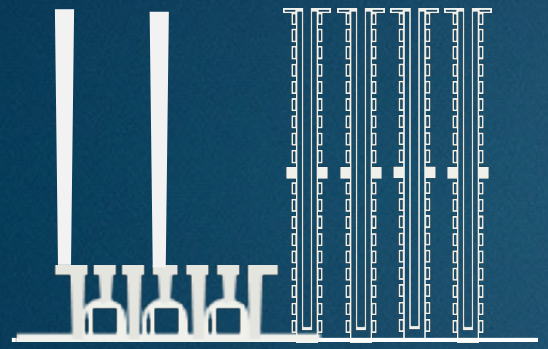
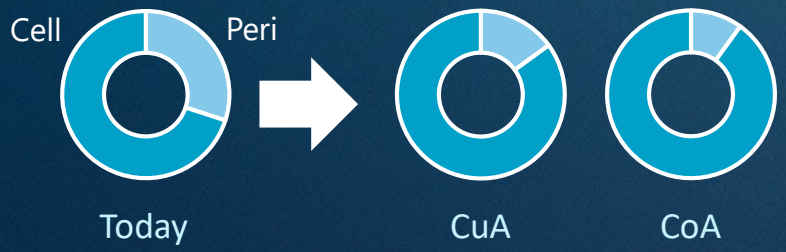
3D NAND CMOS Area Savings

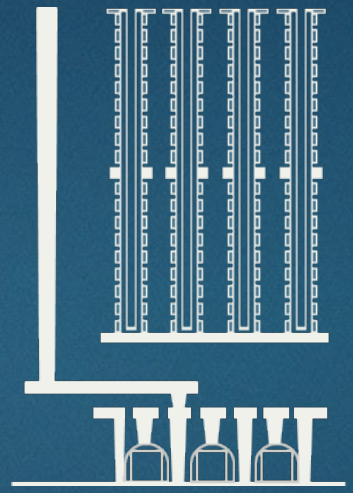
Today's CMOS and array are side by side



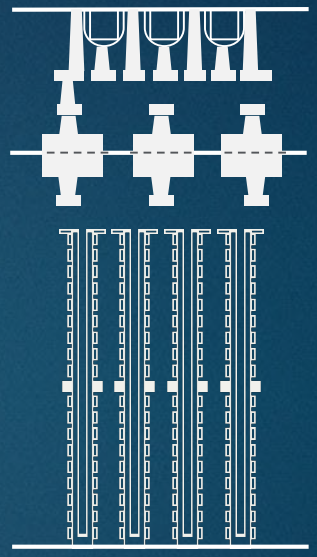
Area ratio



Under (CuA)



Over (CoA)



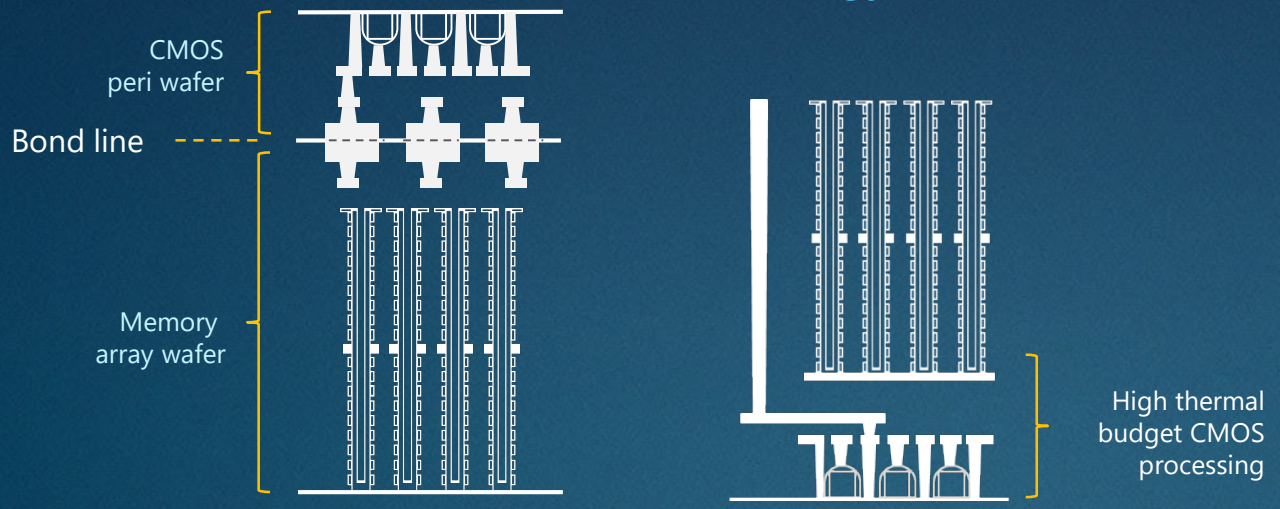
Benefit	Relative low cost	Higher CMOS performance
Challenges	Fabrication thermal budget	Wafer to wafer bonding
New capability required	Specialized implant & thermal Less stress metal fill	More copper interconnects CMP and Die to wafer bonding
Adoption	3 customers	1 customer

Cell – Memory array area
Peri – Peripheral logic CMOS area

Applied Materials External Use

APPLIED MATERIALS

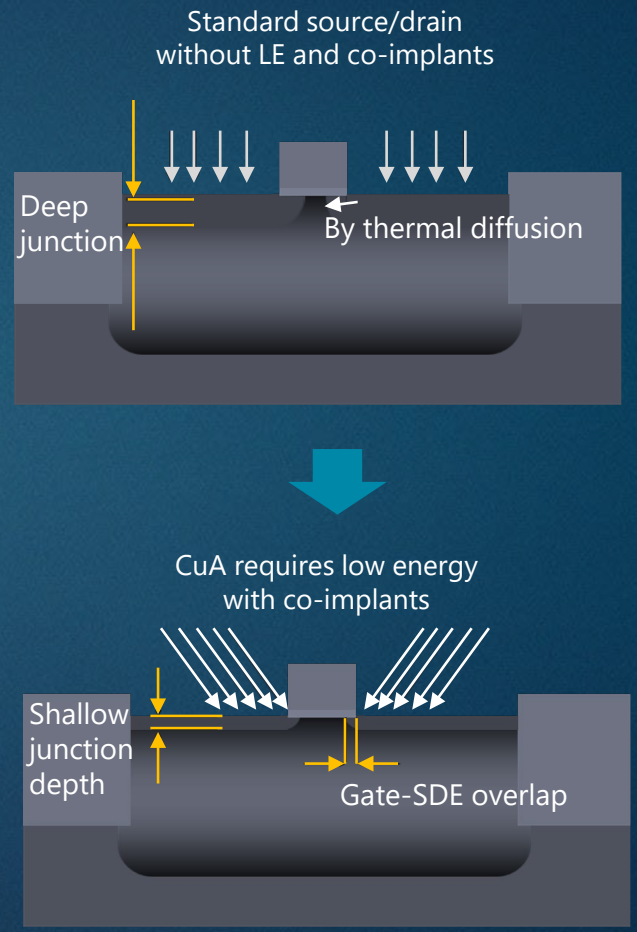
New Process Steps Enable CuA and CoA



Impact to interconnect technology

	Conventional	CoA	CuA
Tungsten	2	1-2	4
Copper	1	4-5	1
Aluminum	1	1	1
Packaging	-	W2W	-

Impact to transistor technology



Applied Materials External Use

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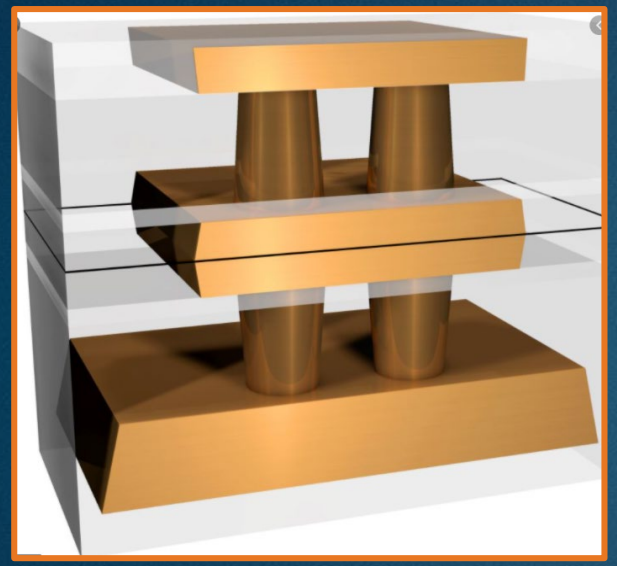
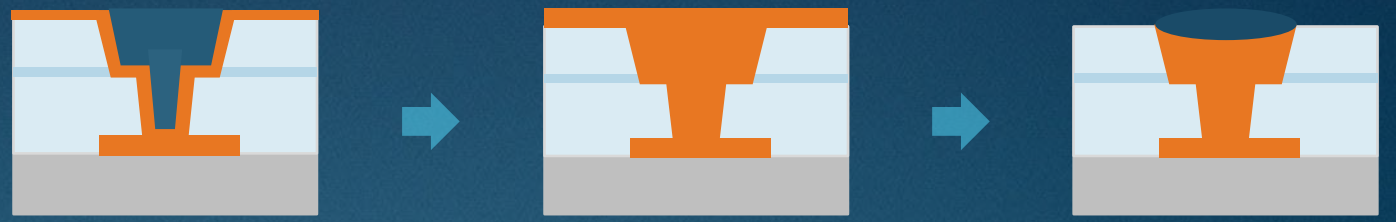
Hybrid Bonding | Enabling Novel CoA NAND Architecture

W2W hybrid bonded (CoA)



PVD: Physical Vapor Deposition
ECD: Electro-Chemical Deposition
CMP: Chemical Mechanical Polishing
WiW: Within Wafer
POR: Process of Record

Key challenges



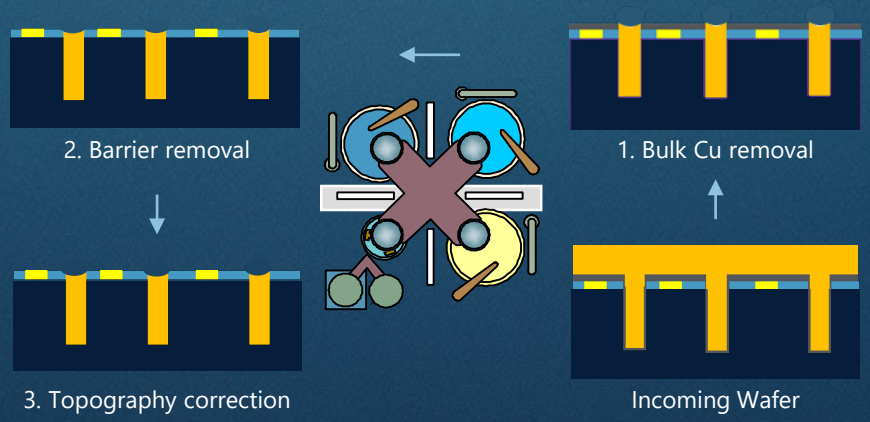
Barrier / Seed PVD

Cu pad fill ECD

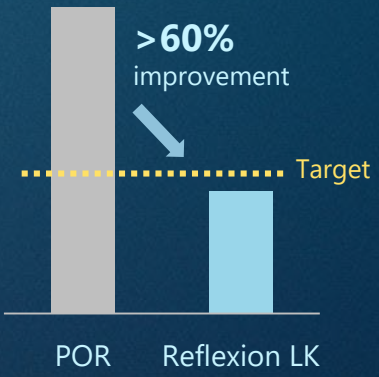
CMP with tuned dishing control

Reflexion® LK Cu CMP

Process optimized over 3 platens



Dishing Range



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Levers for 3D NAND Scaling: Vertical

Scaling lever	Current	Inflections
Vertical	~100p 	>100p + Pairs  >120p - Pitch  >150p + Tiers 

Module	High Value Problems	Solutions
+ Pairs	Hardmask selectivity and etch cost	New Hardmask required Etch cost effectiveness decreases with AR
- Pitch	Removal of SiN and metal fill Pattern collapse	SiN Exhume and ALD Metal High modulus ON
+ Tiers	Complex process, e.g. staircase integration Higher aspect ratio structure	New hardmask and Etch ALD and CVD Fill

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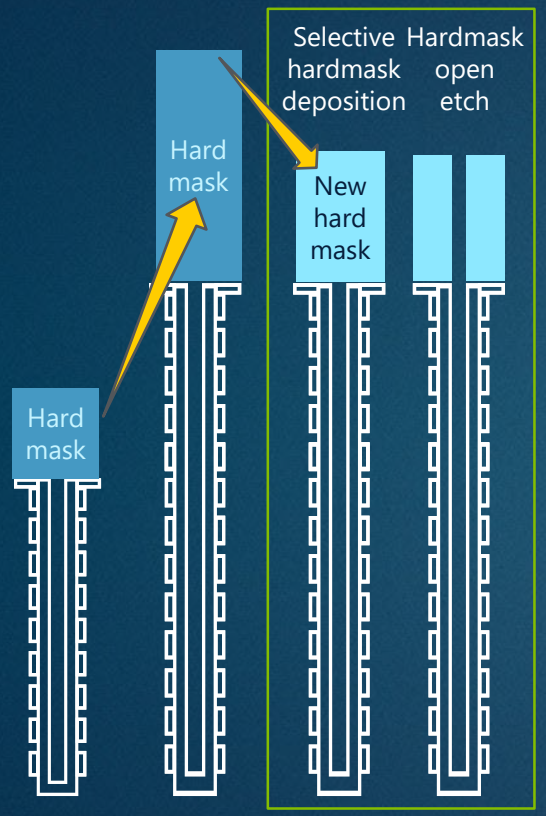
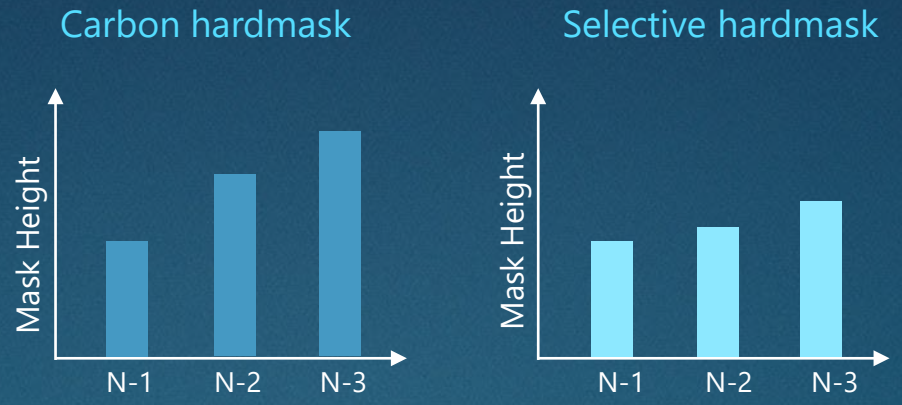
Co-Optimized Hardmask Deposition and Etch

HIGH VALUE PROBLEM



Increasing hardmask thickness

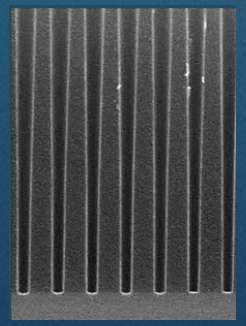
More selective hardmask



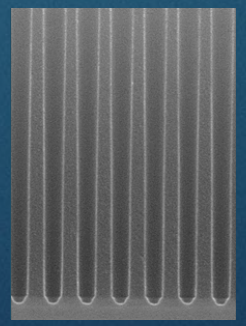
- High selectivity
- Low stress
- Transparent film

Co-optimized hardmask etch

Conventional etch



Advanced etch



- Unique source design
- Improved profile
- Available strip solution

In high volume production for multiple layers

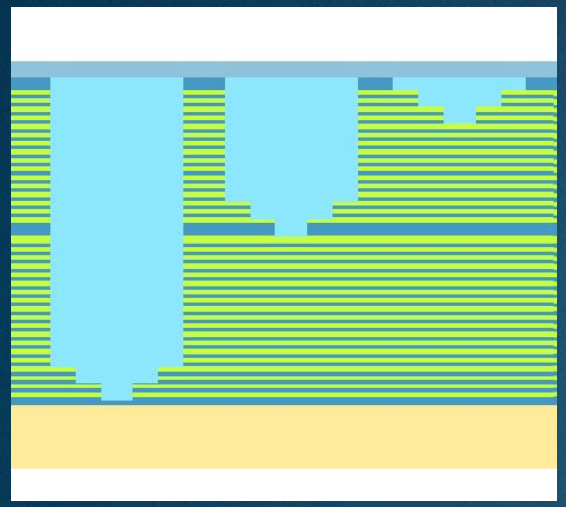
HMO – Hard Mask Open

Source Applied Materials

Applied Materials External Use

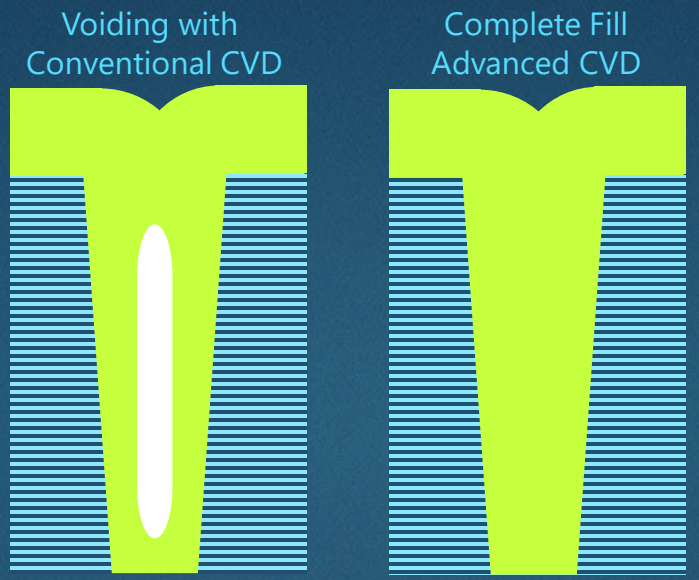
High Aspect Ratio Large Area Gapfill

HIGH VALUE PROBLEM



- Large gaps to fill > 2um
- Aspect ratio > 10:1
- Impacted by shrinkage

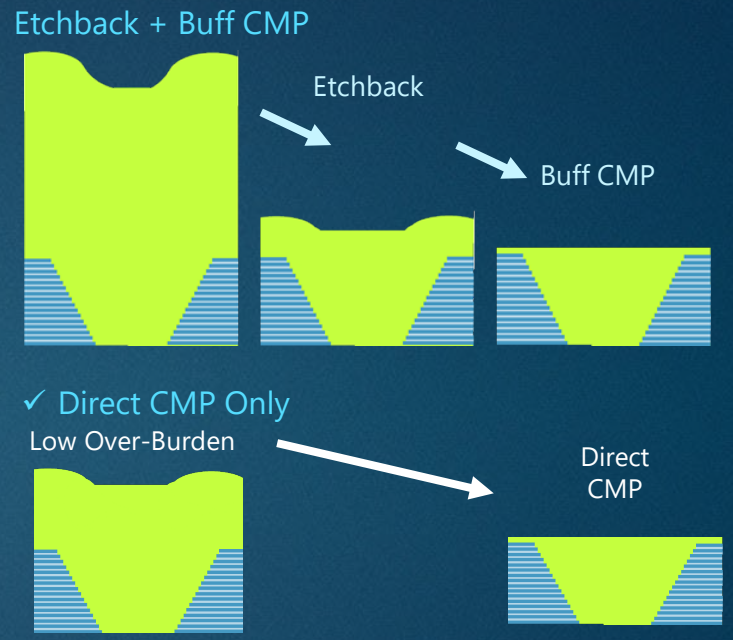
Gapfill oxide



- Low shrinking film
- High deposition rate
- Tunable stress

In high volume production

Simplified planarization



- Excellent dishing performance
- Eliminates etchback step

In high volume production

CMP: Chemical Mechanical Polishing

Applied Materials External Use

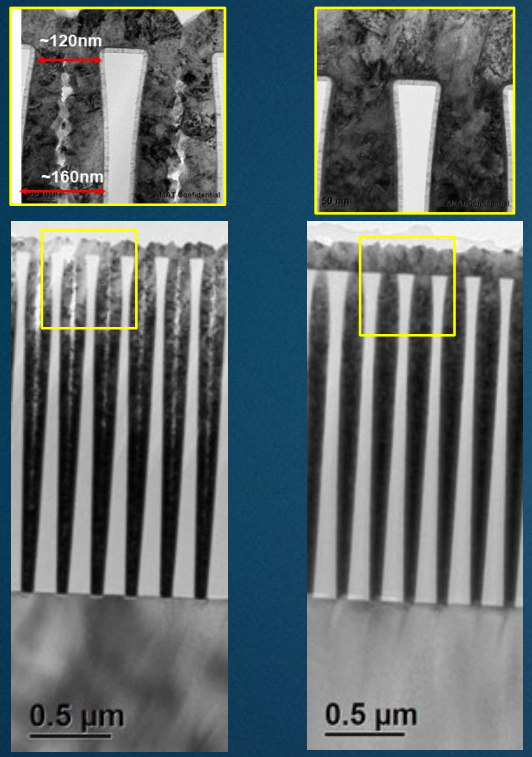
APPLIED MATERIALS

3D NAND Vertical Scaling | Metal Gapfill

HIGH VALUE PROBLEM

Conventional CVD W

Seam suppressed CVD W

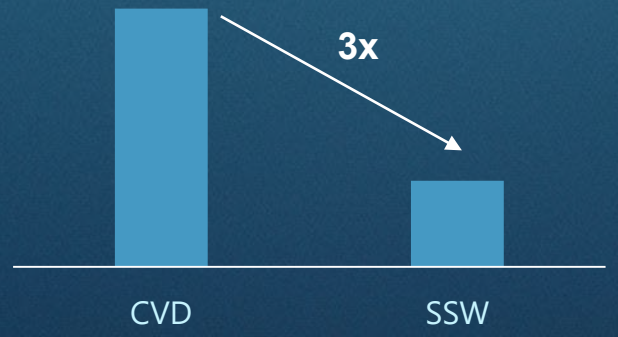


Gapfill voids trap corrosive gas
Tungsten stress damages features

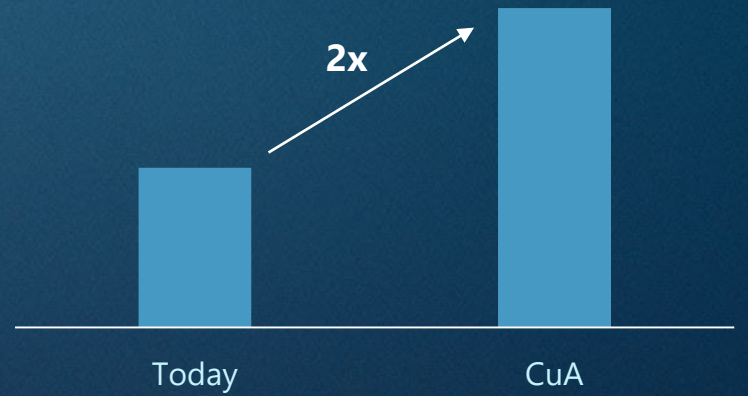
Seam suppressed gapfill

Nucleation | Treatment | Bottom-up gapfill

Low stress gapfill



Step increase with CuA



Source: Applied Materials
SSW – Seam suppressed tungsten

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Enabling PPACt Roadmap for NAND

	256Gb/512Gb TLC		**512Gb/1Tb TLC / QLC**		**2Tb+ QLC / QLC+**
~30L	~70L 1Gbps	>100L	>150L 3Gbps	>250L	>350L >4Gbps
2015	2017	2019	2021	2023	2025

2 Tiers

High AR hardmask dep/etch

Zig-zag staircase etch

Seam suppressed W

Optimized Junction CuA

High selectivity hardmask dep/etch

HAR gapfill, direct CMP

Barrier-less metal

Heterogeneous bonding CoA

Well positioned with leadership products and integrated materials solutions

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make possible

PART 3

Memory Growth Opportunities

Raman Achutharaman, Ph.D.

GVP, Head of Technology, Strategy, and Marketing

MEMORY MASTER CLASS | May 5, 2021

Applied Materials External Use

AGENDA

9:00	**PART 1**	HOST: Mike Sullivan Memory Thesis Fireside Chat | Ed Doller
9:15	**PART 2**	HOST: Kevin Moraes, Ph.D. Memory Technology DRAM | Sony Varghese, Ph.D. NAND | Sean Kang, Ph.D.
9:50	**PART 3**	HOST: Raman Achutharaman, Ph.D. Memory Growth Opportunities
10:00	**Q&A**	Raman, Kevin, Mike

Applied Materials External Use

Significant Momentum Across Device Types

Patterning growth + new products/solutions = Increased memory share, balanced portfolio

Source: Gartner, VLSI, Applied Materials

Applied Materials External Use

APPLIED MATERIALS®

Applied = PPAC*t* Enablement Company

Unit process leadership and broadest portfolio	+	Unique combinations of technologies	+	Actionable insight / time to market acceleration
MATERIALS CREATION, MODIFICATION, REMOVAL, ANALYSIS		CO-OPTIMIZATION INTEGRATED MATERIALS SOLUTIONS (IMS), PACKAGING		ACTIONABLE INSIGHT ACCELERATOR (AI^{X} ™)

Applied Materials External Use

Going Beyond Unit Process Tools to Deliver Solutions

FASTER TIME TO MARKET, HIGHER VALUE, STICKIER

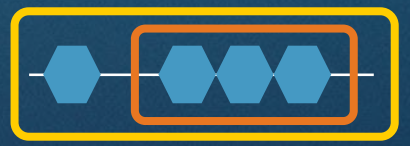
UNIT PROCESS LEADERSHIP
+ BROADEST PORTFOLIO

CO-OPTIMIZATION OF
PROCESSES / TOOLS

~40% of our products
now co-optimized

INTEGRATED
MATERIALS
SOLUTIONS

~30% of our products
now integrated



SENSORS + eBeam + AI / ML

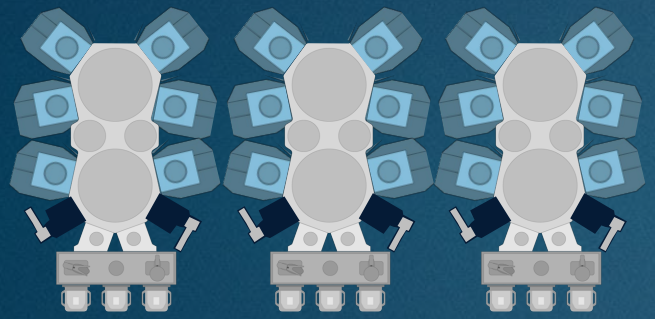
ACTIONABLE INSIGHT
ACCELERATION

New

APPLIED MATERIALS

Applied AIˣ ™ Actionable Insight Accelerator

real-time ability to see into the process with innovative sensors, in-vacuum metrology



Process tools

>10,000 process possibilities per tool
>1,000,000 possibilities per integrated flow

+

massive **actionable data with unique metrology**

PROVision®

100X faster
50% higher resolution

+

AIˣ ™ analytics platform across all Applied tools

- ChamberAI™ ML algorithms
- AppliedPRO™
- Digital twin models
- Integrated controls

Making every stage faster and better: R&D, ramp and HVM
2X faster with 30% better process window

HVM = High Volume Manufacturing

Applied Materials External Use

APPLIED MATERIALS®

Introducing Materials Engineering Solutions for DRAM Scaling

APPLIED MATERIALS®

NEWS RELEASE

Applied Materials Introduces Materials Engineering Solutions for DRAM Scaling

- *New Draco™ hard mask material co-optimized with Sym3® Y etcher to accelerate DRAM capacitor scaling*
- *DRAM makers adopting Black Diamond®, the low-k dielectric material pioneered by Applied Materials to overcome interconnect scaling challenges in logic*
- *High-k metal gate transistors now being introduced in advanced DRAM designs to boost performance and reduce power while shrinking the periphery logic to improve area and cost*

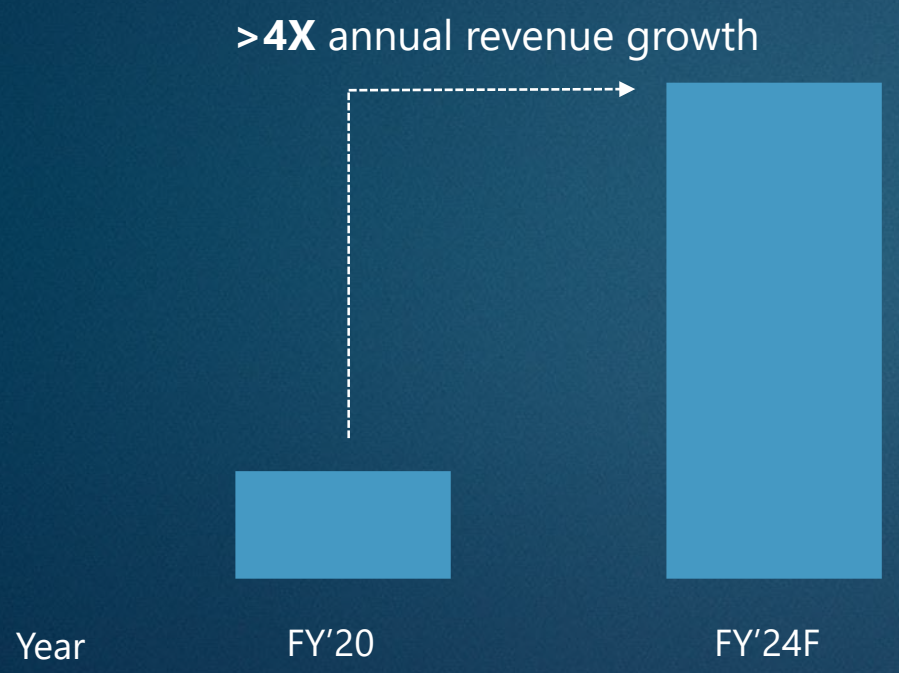
SANTA CLARA, Calif., May 5, 2021 – Applied Materials, Inc. today announced materials engineering solutions that give its memory customers three new ways to further scale DRAM and accelerate improvements in chip performance, power, area, cost and time to market (PPACt).

The digital transformation of the global economy is generating record demand for DRAM. The Internet of Things is creating hundreds of billions of new computing devices at the edge which are driving an exponential increase in data transmitted to the cloud for processing. The industry urgently needs breakthroughs that can allow DRAM to scale to reduce area and cost while also operating at higher speeds and using less power.

Applied Materials is working with DRAM customers to commercialize three materials engineering solutions that create new ways to shrink as well as improve performance and power. The solutions target three areas of DRAM chips: storage capacitors, interconnect wiring and logic transistors. They are now ramping into high volume and are expected to significantly increase Applied's DRAM revenue over the next several years.

Growing by Enabling the Capacitor Roadmap

$1B cumulative TAM opportunity



Breaking tradeoffs: area, capacitance, variability

Innovative technologies + acceleration with co-optimization + acceleration with metrology

Delivering node-over-node PPAC*t* gains
↑performance, ↑yield, ↓area

DTOR / PTOR at major DRAM customers

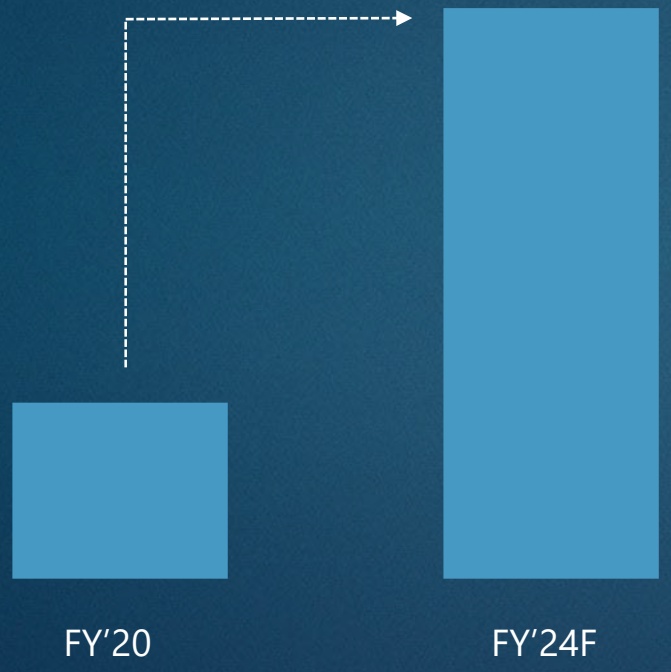
DTOR = Development Tool of Record
PTOR = Production Tool of Record

Applied Materials External Use

Leadership in PPACt Solutions for Periphery Scaling

>$2B cumulative TAM opportunity

>3X annual revenue growth



Leadership products for HKMG transistors and interconnects

Decades of experience with logic-like processing

Delivering node-over-node PPAC*t* gains
↓power ,↑performance, ↑yield, ↓area

DTOR / PTOR at major DRAM customers

DTOR = Development Tool of Record
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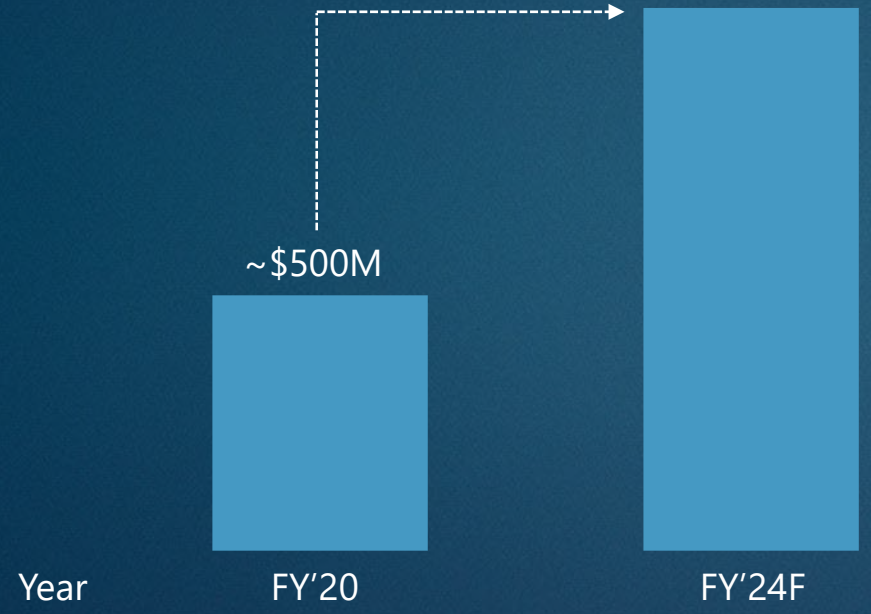
Well Positioned for Growth in Packaging

Early innings of multi-year growth



#1 in bond-pad, bump and TSV

Broad product portfolio + full-flow lab

Key eco-system partnerships

Delivering system level PPAC*t* gains
↓ R, ↓ power, ↓ area, ↑ performance

TSV = Through Silicon Via

APPLIED MATERIALS®

TAKEAWAY
Messages

1. 'AI era' = **Secular growth** and accelerated innovation
2. Applied = The **PPACt enablement** company
3. **Uniquely positioned** to accelerate the PPACt roadmap
   Unit processes, unique combinations, actionable insight acceleration
4. Multiple big **inflections and growth opportunities** for Applied Materials

* Free cash flow = operating cash flow – net capital expenditures
** Non-GAAP adjusted EPS

Applied Materials External Use


APPLIED
MATERIALS®
make possible